Deep Science Publishing
https://doi.org/10.70593/978-81-989050-5-5_1

DeepScience
Open Access Books

Chapter 1: Reimagining microelectronics: Evolution and future potential of modern circuit design paradigms

1.1. Introduction

Microelectronics is perhaps the most influential and impactful engineering field in the modern era. The concepts and applications of integrated circuits have expedited the continuous growth and prosperity of computer science, communications, signal processing, control systems, as well as numerous other foundational technologies that affect daily life quality and economic progress on our planet. Following the analog circuits in the first two decades, which were the foundation of the early microelectronics era, the impressive achievements of microelectronics mainly came from the continuous pursuit of digital integrated circuits. Starting from the 1980's, the advances of digital microelectronics sparked thriving innovations in computer chips and revolutionized personal and mobile computing, information processing, and communication (Das & Kumar, 2025; Hernandez et al., 2025; Kim & Rao, 2025). The future of microelectronics is filled with thunder, however. For the first time in decades, the law of doubling the number of transistors on an integrated circuit per unit volume every two years has reached a critical bottleneck, and a slowing down is inevitable in the advancement of digital microelectronics technology. At the same time, many new and innovative small form-factor applications and products are emerging. Unlike traditional desktop computers, the future products and applications are mostly designed for distributed smart computations at the edge with continuous AI workload. From electrical power consumption, mobile battery life, cost, thermal management, to ease of hardware and software integration, and real-time responsive performance, unprecedented challenges are presented for component and system design of the new generation smart products and applications. More than ever, innovation in microelectronics technology and circuit design paradigms is of vital importance for empowering the ever-increasingly capable smart functionalities at the intelligent edge to meet global demand of the next decade (Li & Singh, 2025; Zhang & Patel, 2025; Kim & Rao, 2025).

1.1.1. Background and Significance

Microelectronics has changed the lives of humans. Even the most mundane and basic of our daily tasks rely on circuits embedded into microelectronic chips, be it sending a text message to friends, depositing money from an ATM machine, or booking tickets by connecting to the Internet. Most of these chips which undertake the complex task of performing billions of transistors manipulations every second, are fabricated using the Complementary Metal Oxide Semiconductor technology, a technology with three major advantages. First, CMOS chips draw smaller amount of power compared to chips fabricated using other designs or technologies. Second, they are extremely reliable when compared to chips fabricated using other designs or with other technologies. And third, they are extremely cheap to manufacture in bulk.

With the significant reduction in chip area yet an increasing number of transistors on a chip catering to the increasing computing needs of the user, the performance of CMOS technology has been scaling per Moore's law with regards to performance for more than five decades and revolutionized human life. Because of the critical and omnipresent role played by microelectronics in the daily life of humans as well as its growing domination in everything from defense systems to social infrastructure, current research trends in the field of microelectronics design are directed towards addressing challenges posed by the three major limitations of the existing CMOS technology. These are: 1) surpassing performance and power ceiling achieved by classical scaling, 2) design flexibility corresponding to more and more diverse requirements and 3) System-on-a-chip integration of more complex multi-core, heterogeneous circuits involving the inter-chip and inter-core communication overheads. As such we need to reimagine modern circuit design paradigms by evolving their potential. In this chapter, we focus on evolving modern circuit design paradigms and reimagining the circuits in order to overcome the challenges with their proper integration and design methodology.

1.2. Historical Overview of Microelectronics

Microelectronics is an area of modern technology founded on the discovery and development of solid-state semiconductor devices that are so small that they require the use of photolithography methods for their fabrication. The emergence of microelectronics marked a departure from existing technologies dealing with coating and positioning materials with sizes within the micro and nano range. On one hand, the technology did not build upon the subsequent application of the semiconductor device

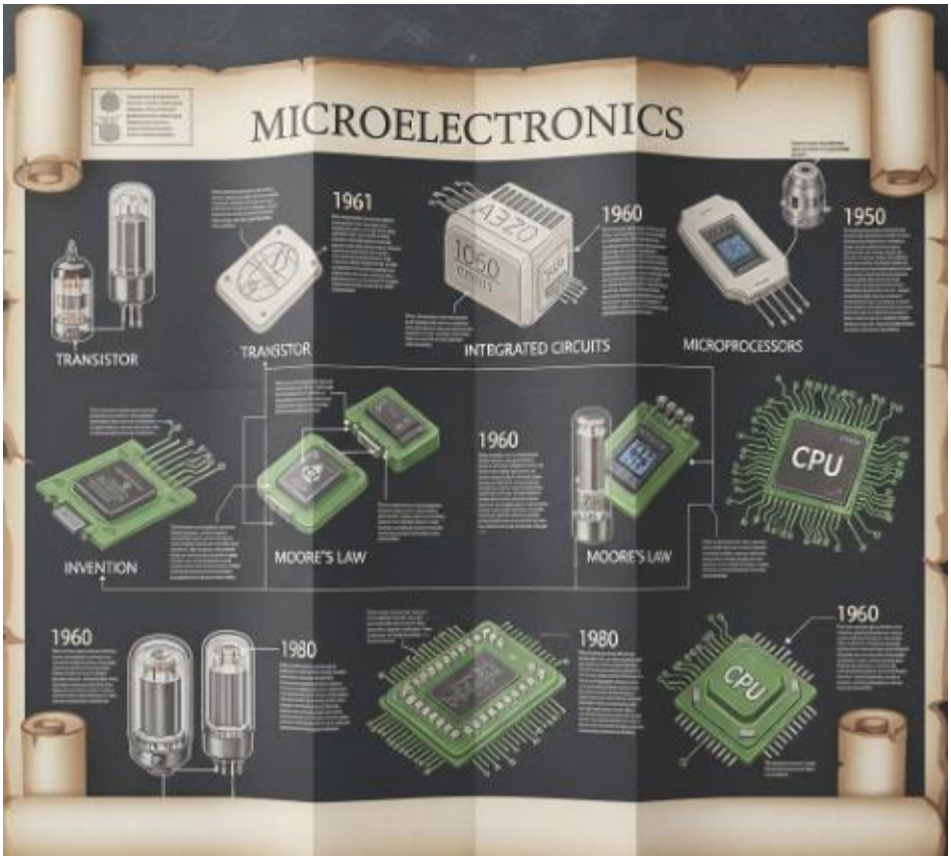

Fig 1.1 : Historical Overview of Microelectronics.

principal, discovery, and applications attributed to pioneers. The field grew from the optical and other physical technologies fundamentally applicable to the design and fabrication of integrated semiconductor devices and circuits. The technology of microelectronics allowed devices to be produced with a size so small that a micrometer scale device and structure had hundreds of times more functional elements and devices within the same area compared to the previously available macro and meso scale technological capabilities, notably including vacuum tubes and earlier technologies.

The first patents for the photolithographic-based fabrication of arrays of devices such as semiconductor device memories were granted in 1959. Photolithography permitted patterning of device sizes, and hence allowable critical dimensions, within the micro range of approximately one micrometer and larger in a process that was integrated with electrochemically aided vacuum metal evaporation and relatively less sophisticated metal and oxide layering and diffusion process patterning and removal processes. Punched card patterning methods had already allowed limited integrated device size capabilities, as had scribing and cutting glass wafer with a diamond. These earlier methods were, however, essentially serial and unable to deposit or mask a device array

over even a small substrate such as a 4-inch wafer within reasonable limits of time required for mass production of devices.

1.2.1. Early Developments in Circuit Design

The history of microelectronics dates back to the day in which a piece of silicon was shown to be able to sustain voltage and carry a current. However, some time went by before practical uses of this newest addition to the electronic components were devised. The invention of the integrated circuit laid to rest the question about the viability of silicon as the foundation of microelectronics. However, creating the building blocks of microelectronic circuits was not enough. To catalyze the explosion of microelectronics triggered by the integrated circuit, practical designs that took advantage of dedicated computer programs had to be produced. This section is devoted to recount the long history of the development of practical design algorithms and tools, starting from the early attempt at designing integrated circuits and systems in the late 1960s. While our focus in this short chapter is on computer-aided electronic and circuit design, it is unarguably the case that early designers were talented in the art of circuit design and relied on creativity and experience, as well as the support of a cadre of hardworking engineers and technicians.The design of solid-state circuits began well before silicon was established as the material of choice for microelectronics. The specifics of solid-state two-terminal devices coupled then with their three-terminal counterparts, the junction bipolar transistors, combined to provide the basic foundation for the design of integrated circuit functions. The observation of the Zener effect of semiconductor pn-junctions in the late 1930s led to two-terminal silicon devices with power capability that were well designed for many electronic functions. The design of diffused silicon integrated circuits was a development effort of many years. Most systems at the frontiers of technology in those early days were based on circuit designs that employed small prefabricated blocks and therefore never made it into integrated circuit fabrications.

1.2.2. Advancements in Semiconductor Technology

Many of the unique properties of semiconductors, needed for IC fabrication, were discovered by the 1940s. The unexpected ability of Ge and Si to work as a rectifier and amplifier were explored since its early days. Many of the basic physics that enables these special features were understood and explained. An important step in the semiconductor development was the release of the p-n junction from laboratory conditions. From then on it was clear that the building blocks needed to produce practical electronic devices had become available for practical engineering work. By the late 1950s the transistor became reliable, cheap and versatile. Diffused-junction transistors made using Si wafers

were invented and patented. Diffused-junction Ge transistors are still available today. The first tunnel diode was a simple Ge p-n junction with a heavily doped n layer, developed in early 1957.Introduction of Metal Oxide Semiconductor (MOS) devices was a major boost to the use of electronics as building blocks for many systems because these devices combined low voltages and power with high packing densities. Improved fabrication techniques led to the production of ICs, including CDAs and Digital-Logic ICs. Later advances led to the combination of both types of functions in the same IC. Considerable efforts went to the design of power and high-frequency applications of Si bipolar ICs to maximize the advantages of this technology, which were low cost and compactness. But of equal importance was the development of the functional modeling and design support systems that have now reduced the time for design of complex ICs to a few weeks using high cost computerized fab techniques.

1.3. Current Trends in Circuit Design

Advances in microelectronics devices and circuits continue at a breathtaking pace but now involve more than just scaling the dimensions of transistors in silicon. AI, machine and deep learning algorithms have made their way into the synthesis of the devices themselves as well as into the CAD for designing complex circuits and the tools to simulate their behavior. New materials are being explored as possible replacements or enhancers of traditional silicon based semiconductor technology. A societal demand for sustainable energy and energy usage throughout the technology cycle is impacting microelectronics as it is many other disciplines. New methods, novel designs, different energy sources for operation, and enhancements to deliver the needed circuits and systems with the lowest possible environmental impact are being explored. All of these trends offer both challenges and opportunities for students and engineers in nanoelectronics.CAD tools were originally developed by people with a strong educational and experiential background in microelectronics, circuit theory and application. Only in the past few decades have design tools with little basis in practical applications been produced. There are critical needs in both areas, for skilled designers with no experience using 3D devices and for developers whose tools are designed for special circuits only. Accelerated answers, while needed, reduce the opportunities for innovation, especially at the device and circuit interaction level. The push for miniaturization, electrification, increased functionality, improved energy performance and new capabilities is using all of the new conceptual possibilities. By exploring the points raised, new designers will be able to prepare not only for the challenges of today, but also for the possible new approaches to the new capabilities that will be needed tomorrow.

1.3.1. Integration of AI in Circuit Design

Artificial Intelligence is helping in solving many problems in the Circuit Design Process, examples range from Logic Synthesis and Optimization, to Placement and Routing, to the generation of the Circuit and Layout in Wafer Scale. AI methods can perform the task with 2 to 5 orders of magnitude lower computational cost (and in some cases solving problems that were impossible to be solved by classical methods due to the excessive computation time). It is estimated that more than 2 million chips per year are fabricated, and the design process for these chips can consume between 10 to 25% of the total costs, so the savings associated with using AI in Circuit Design has a huge impact in the industry. On the other side, one of the main problems is the need of having a large dataset for training purposes, and also that the training stage takes a significant amount of computational resources to be achieved, nevertheless large companies have been able to achieve efficient designs using AI.

Even more, semiconductor companies are also looking for other methods that go beyond DNN using DQM, or Reinforcement Learning. Also methods that combine classical circuit methods with AI are being explored. By DoE, an efficient method for different types of Circuit Design problem has been presented, and it consists of 3 phases: Parameter Setting, Transfer Function Development, and Optimization. DoE is a systematic, statistical technique that is used for designing and analyzing experiments. The aim of this framework is to provide a strategy that can answer a set of parametric questions with the minimum number of experiments.

1.3.2. Emerging Materials and Their Impact

The demand for more efficient and faster electronic devices has fueled extensive research into obtaining better resources in terms of improved materials and processing technologies. The traditional transistor architecture operated by silicon MOSFETs has been followed for the last six decades, and the use of silicon-based technologies, from the device to the board level, has been highly successful. However, despite its many advantages, Si has difficulties in satisfying the requirements of the future generations of electronic devices such as speed, power, area, and costs. From a materials perspective, the key innovations in current CMOS technologies have been the introduction of high-κ dielectrics, metal gates, and strained Si channels. However, the end of the silicon era might harbor the potential for substantial heterogeneity in integration solutions enabled by new materials, concepts, and technologies. These might include new transistor architectures, as well as the use of lower-dimensional materials and the hybrid integration of disparate platforms at the nano- and micrometer scale.

In particular, the advent of novel lower-dimensional materials, such as transition metal dichalcogenides, as well as the hybrid integration of disparate platforms, might allow realizing new functionalities unachievable until now. New III-V, II-VI, and other low-bandgap semiconductor materials on silicon or heterogeneous integrated platforms could be used for optoelectronic devices capable of novel functionalities. Atomistic device simulations in augmented spaces will provide the theoretical support to guide this exploration. In this chapter, we will briefly outline some emerging materials or material platforms with potential disruptive implications for integrated circuits of the next ten years and beyond. The focus will be on the materials themselves as well as on potential circuits and applications enabled, not so much on NWs or the two-dimensional limit.

1.3.3. Sustainability in Microelectronics

Sustainability is generally not in the scope of efforts in microelectronics when the priorities are always and mostly followed by performance, energy, and area efficiency. There is a considerable irony in this. Microelectronics is undoubtedly responsible for the tremendous advances of other fields of modern technologies in energy, health monitoring, and data management, helping create a society that effectively uses technology to lower the carbon footprint. Despite these indirect layers of improvements that make the world more efficient, the microelectronics industry does not directly participate in reducing its own impact using energy wisely and sustainably, when creating the circuits, chips, sensors, etc. The microelectronics industry is largely responsible for the exponential growth in energy consumption, while the chips created are made to support this trend as plugin devices and mobile and wireless devices while never stepping down to consider the impact of their existence, and above all, the actual costs of supporting the massive consumption of energy required during the fabrication of each device, the cost for the environment incurred in their disposal, and the loss to the industrialized countries who have traded their dependence on fossil fuel with that on rare earth that belong to third world countries. There have been ongoing efforts into the green electronics space, related to energy-efficient circuit design, low-voltage logic designs, miniaturized and embedded systems. These efforts are either related to the design or operational efficiency during usage. Little consideration has been given to how to design these circuits in the first place.

1.4. Design Paradigms in Modern Microelectronics

Development of a computer-aided design tool is a tedious process that requires implementation of discipline and spending of huge resources. New design paradigms in microelectronics remove the gap between potential of new technologies and digital

design methodologies used so far. It is no longer desirable to continue design systems and methods that have been developed in response to the reality of the design economy of the past decades. The design paths need to be cleared for the incorporation of new technologies into chip and system design. Removing the old habits and entrenched philosophies will not be easy in any area of design: CAD usually has the last words in design methodology. But it is increasingly clear that the powerful new solutions being made possible with advanced technologies will not be implemented without serious deposition of efforts in CAD and serious collaboration between designers and CAD architects.

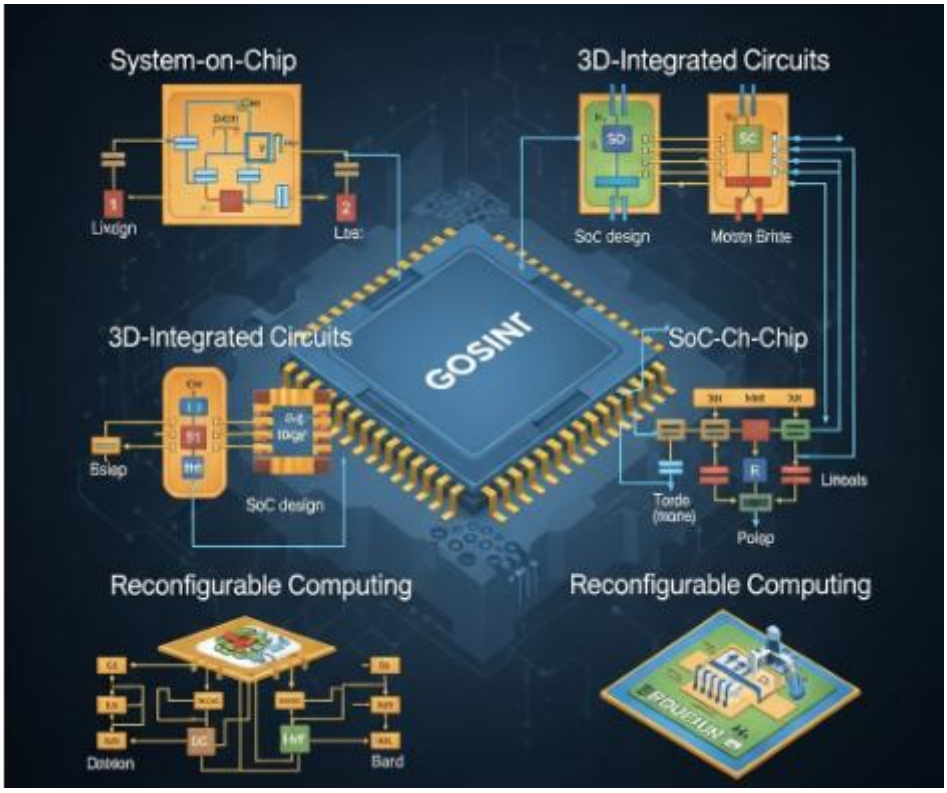

Fig 1.2 : Design Paradigms in Modern Microelectronics.

Some of the traditional design approaches that are often impediments to substantial productivity or efficacy improvements include design automation that is at least one step removed from actual design methodology. Designers have traditionally been able to rely on libraries of designs, devices, and cells to speed the design process and the use of these tools increases user throughput with assumed design attributes. Novel design elements include cell multiplexing, which allows designers to continue to automate functions with current reduction, while taking cell replacement out of the reach of static tools. Emphasis on clock period reduction rather than simple speedup in some traditional analysis

assistance. And design support libraries with device models that can be used in custom design and tools for more interactive layout flow without major penalties in routing predictability and manufacturing accuracy.

Departmental or corporate-wide design rules for basic rule-based congestion estimators for design assistance during the early phases of block floor planning before full chip layout. And new levels of design documentation for the design community, which are essential to enable simultaneous design of the custom or semi-custom integrated circuits and the digital and analog building blocks of the digital circuits.

1.4.1. Traditional vs. Novel Design Approaches

Traditional circuit design approaches mainly require skilled engineers to work in a top-level-down approach realizing increasingly detailed and complex symbolic circuit diagrams or logic equivalence transformations arriving at deliverable netlists for fabrication. Whether designing a class of circuits with highly-individualized performance needs or designing analogous circuits in massive volume production, this highly-manual effort has been the heart of the circuit design approach. However, in modern digital societies, products need to respond to lifestyles that form and change rapidly, thereby reducing acceptable time to market and increasing variety. In addition, many products that utilize complicated logic are usually not conveniently mass-producible in large volume and large volume production requires that these products also take on various specializations, creating an even higher demand for reduced time to market. This criticality to product time to market is the need to utilize long-tailed strategies rather than just a hit producing winner-take-all strategy of product design. Not only are products tailored but the cycles of design and adaptation that respond to change are reduced so that rapid innovation becomes part of the ecosystem that encourages, facilitates and leverages product and design change, emergence and innovation. The gentle art of Engineering, especially in the design and practice of Function itself, must give way to the rigidity of Constraint by which thought and action must conserve the resources of Time, Property and Possibility most effectively. The gradual need to utilize arrangements of ever increasing complexity in Electronics is evolving a novel paradigm for design in its responsible and conscious application of Dualism, in its architecture that takes on the spirit of Constraint, and in its philosophy of conceptually realizable, yet programmatic and proscriptive structures.

1.4.2. System-on-Chip (SoC) Architectures

Embedded systems have pervaded contemporary consumer and mobile electronic markets, leading to the mass production of System-on-Chip circuits integrating digital

logic with analog functions like RF transceivers, phase-locked loops, and analog-to-digital converters. In SoCs, novel memories like suspended-gate flash, magnetoresistive RAM, and ferroelectric RAM allow the incorporation of non-volatile memory with logic for paste-on-probe solutions. Numerous problems abound, however. From a logical point of view, existing parallel architectures are not easily scalable. This is due to mutual contention for shared area resources, routing congestion, and low computability of widely adopted embedded central processing units.

From a thermodynamic point of view, the tailoff of diminishing returns has rendered the steady-state computation efficiency of arithmetic devices relatively low. In the presence of increased demand for energy-efficient computation, embedded systems can benefit from the use of specialized process technologies and circuit implementations. These consider unique application needs such as battery reconstruction and energy scavenging while providing protection against electromagnetic interference. Counterintuitively, these optimized trade-offs could ignore manufacturability and yield, yet permit the construction of monolithic USB-compliant cables that bypass bulky filters and high-speed differential signaling for reduced energy expenditure. Integration of these specialized devices within a comprehensive SoC framework that utilizes traditional programmable elements for general-purpose computations aims to maximize energy efficiency.

1.4.3. 3D Integrated Circuits

The journey toward microelectronics and optical devices miniaturization has been accompanied by a search for ever-serrated integration processes. These challenges rely on developments and solutions on new technological and design paradigms. The concept of three-dimensional (3D) integrated circuits (ICs) has emerged as a powerful solution to overcome the increasing constraints in traditional two-dimensional IC structure scaling. 3D ICs vertically connect multiple devices, thereby reducing wire length and increasing performance density. 3D ICs can be fabricated as a stack of partially processed dies or layers or a true 3D fabric through direct epitaxial growth. 3D ICs constructed with silicon layers or dies are connected through vias in the oxide dielectric layer stack between the chips and solder bumps or micro bumps, such as copper, through silicon vias, and metal pads.

Short communications links bring many excellent features, such as low power consumption, significant performance improvement, and ultra-low interconnection time delay. Additionally, 3D ICs can exploit the fabrication of heterogeneous integrated circuits. Such circuits can take advantage of both front and back-side access technology accuracy on different paving building blocks or functional layers. More specifically, 3D ICs can integrate digital, analog, RF, embedded MEMS, and power devices. These

technologies allow for true 3D circuits utilizing the CMOS process and the same material, Si. A true 3D heterogeneous Integrated Circuit (IC) can be achieved through an epitaxial transfer process. Notably, a real 3D IC has several major advantages compared with a 2D IC. First, true 3D ICs and epitaxial stacks permit avoiding the metal interconnect, which is the main cause of performance degradation, on 2D ICs.

1.5. Challenges in Circuit Design

Circuit design is a narrow yet crucial aspect of microelectronics development. Its impact has been felt in changing circuit design paradigms to address loss of performance scaling as well as imaging novel uses for microelectronics as an efficient and low-cost technology for an incredibly wide array of applications. Circuit design is applied to very diverse applications ranging from nanoelectronics to analog and RF circuits, to high-speed data converters and mixed-signal systems, to power and electromagnet circuits, to low-power biomedical integrated systems. These are applications used to process information by accumulation and evaluation of incoming signals. In this chapter, we discussed some important circuit design challenges encountered in modern circuit design paradigms to promote novel applications of microelectronics, and pointed to possible solutions. Issues encountered relate to thermal management, power consumption and energy efficiency, as well as design for manufacturability and test.

One of the challenges of integrated circuit design is the need to minimize the power consumed by the chip to maintain reliable operation in a compact physical area and prevent heating above specified temperatures. This challenge is especially important in circuits used in portable applications because of the deterrent effect to use of these electronic devices for prolonged periods of time. Yet the internal power of many integrated circuits has increased considerably due in part to the increasing number of functional elements in these devices, and in part due to the need for high speed operation to service the increasing application demand for higher data flow rates and bandwidth. With today's technology, it can be shown that it is becoming progressively more difficult to meet reliability specifications due to excessive temperature levels.

1.5.1. Thermal Management Issues

Current and projected silicon technology scaling has accelerated circuit performance improvement. This, however, greatly complicates circuit thermal management. The thermal management challenges at the basic circuit level are exacerbated at the chip level, given the restrictive limits for chip package thermal resistance. Due to the growing thermal limits, the power density, integrated area, and time required to dissipate the heat from a chip module have reached levels that threaten device life and further improvement

in overall chip performance. The growing chip hot spot temperature threatens not only the reliability of the chip during its conventional operation but also its functionality during under- and over-execution.

Thermal management issues are not recent concerns in circuit design. Different thermal sensitive circuit design techniques have been proposed in the past few decades. These thermal management techniques have implicitly or explicitly been integrated in the general design flow. There exists an extensive volume of work on thermal management that can generally be divided into device placement and routing techniques and dynamic and static thermal management during circuit operation. Thermal manufacturing strategies include cooling, heatsinking, fan operation, and active thermal management. Thermal management has primarily been limited to the physical level, with thermal profiles being in some cases investigated and accounted for in the design process, and adjustments made to placement, routing, and thermal vias to passively address chip thermal performance problems at a late packaging stage. In this chapter we will focus on the circuit solutions for circuit speed, dynamic and static power saving, and thermal performance imbalances of design, which can also be considered chips thermal management information that are usually incurred at later design stages with little refinement capability.

1.5.2. Power Consumption and Efficiency

As described in Section 1.4, traditional circuit design approaches focus on providing higher performance while observing the specifications of the corresponding physical layers. Even with this approach, dealing with power and efficiency costs is difficult. The performance of a given design shows an inverse-square relationship with the power supply voltage; therefore, reducing supply voltages is one of the techniques used to reduce global power dissipation. Nevertheless, this requires a decrease in the speed at which each transistor switches to achieve the standard delay time, which is accomplished by either sizing up the transistors or relaxing the specifications of the transistor model used. Leakage power dissipation (especially subthreshold leakage) has also become a major problem for both large and small designs, e.g., microprocessors and SRAM devices. Gate-based and RD-based leakage reduction techniques create a threshold-voltage variation that becomes a significant challenge for both circuit-level and physical-layer designers. The problems associated with ON/OFF control for extreme low power also limit the speed of circuitry designs at ultra low supply voltages. Furthermore, in some designs, for example, RF and analog circuits built with the same technology, the difficult RDs used to reduce leakage increase the gate capacitance, which reduces the amplification gain, finally yielding RF circuits with poor performance. The above methods could help substantially lessen the total power dissipation of a technology, but

what is becoming more important is the improvement in energy efficiency, i.e., how efficiently a technology can consume energy. Considering that performance increases per transistor will be half every 18 months, if we had had to choose between high energy-efficiency designs and high-speed designs without consideration of design complexity, we would have selected high energy-efficient solutions. However, the reverse triangle relationships between energy and speed still hold, meaning that reducing energy costs means sacrificing speed.

1.5.3. Design for Manufacturability

Design for manufacturability (DFM) is an important consideration at the circuit level due to the increasing influence of process variations on overall device performance characteristics. In advanced technologies, lithography, etch, and deposition process variations dominate the random component of threshold voltage (Vt) variations. Design practices to minimize the effects of these process variations on random Vt fluctuations, such as reduced Vt sensitivity, critical dimension (CD) control, and alignment sensitivity, are known as DFM techniques. DFM is often viewed as a physical design (layout) issue, but it is also a very important consideration at the circuit design level. In the digital realm, cell design influences on circuit-level DFM requirements include impact on the device mismatches, random Vt modules package mismatch correction, ESD cell design, CD controllability through choice of the Vt parameters and substrate voltage control, cell impact on placement density, number of gate contacts and design parameter chosen, correlating elements, multiple contacts design, and aspect ratio. The knowledge of technology design rules and design packaging delays and drivability requirements and impact on speed, signal integrity, and power consumption must also be considered.

Design for manufacturability is a process in which specialists from design, process technology R&D, and manufacturing teams cooperate during the design phase of a chip development flow to identify the limitations of each of their processes, and to subsequently converge on a design configuration that considers these limitations, thus minimizing the risk of cost overruns for design changes, silicon retesting, and mask redrawing. DFM is team effort starting with SIP PhD vs. MAT PhD degree holders, thereby involving trading off sensitive design specifications that would require adjunctions in the flow proposed, thereby requiring more time, during routing, and Vt assigned, thus deciding on the design rules to be adopted for the intended device period of operation. This is particularly challenging because of the differences in underlying process technologies between digital and analog design.

1.6. Future Directions in Microelectronics

The continuous research work worldwide helps in discovering novel architectures and device combinations that could deliver efficient solutions to solve the problems of the modern computing paradigm and electronics industry. These alternative approaches give rise to what many are calling "post-Moore's Law" solutions to the end of density scaling. These next-generation schemes must borrow from more than the just traditional semiconductor roadmap if disruption is to occur. Disruptive advances in advanced circuit design techniques, innovative architectural designs, new emerging device technologies, design for manufacturability techniques, and heterogeneous integration methodologies are all necessary. This session will highlight a unique mix of research and implementation work focused on addressing macro and micro issues of the continuing challenges in circuit design in small scale and beyond. Therein we will discuss more than the just continuing importance of devices circuits and systems in solving the ever-growing problems of efficiency and implementation in microelectronics.

The concept of computing has remained unchanged since the beginning of the computer age, with the idea of a digital computer a universal tool for computation being a persistent object with the general tendency of miniaturization at a rapid pace. However, there have been challenges heralding the apparent end of Moore's Law. The increase in computational speed that can be achieved, and the diminishing of the costs related to the computing activity that can be obtained have continuously depended on per capita income growth and the unprecedented increase of solid-state computer power of about one billion times, with increases constantly doubling every few years. The continuous unending demand of the various computing and electronic applications has always spurred the innovations in what was called the microelectronics industry from the basic building blocks like semiconductor devices to the sub-system, and now to the system fully integrated into electronic products.

1.6.1. Quantum Computing and Its Implications

Quantum computing is an extraordinary technological breakthrough that promises to solve problems that classical computers either cannot solve or take an unreasonable amount of time to solve or both, thus revolutionizing many fields of human experience: for instance, cryptography, medicine, material science, machine learning, and the development of Artificial Intelligence. The secret behind quantum computers is that they exploit and take advantage of quantum mechanics, the laws that govern the behavior of the smallest constituents of matter. While bits, the building blocks of classical computers, can only take two values (0 or 1), the qubits, the building blocks of quantum computers, can take others, thanks to the capacity of quantum mechanics to exist in a state of superposition. Qubits can also be strongly correlated to each other, thanks to a

different effect of quantum mechanics: entanglement. These two characteristics allow quantum computers to surpass classical computers in terms of performance.

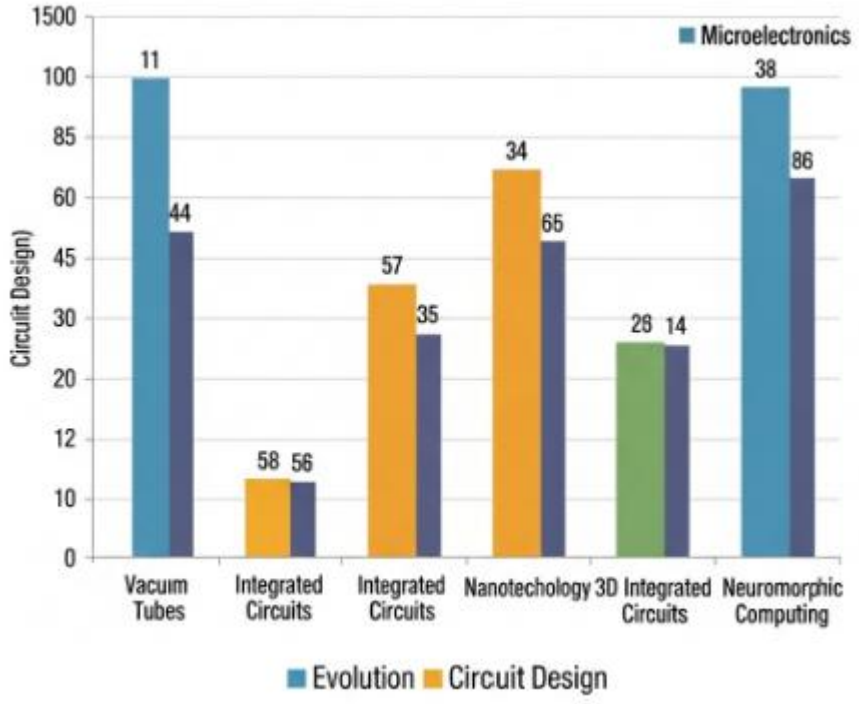

Fig : Reimagining Microelectronics: Evolution and Future Potential of Modern Circuit Design Paradigms.

Quantum computers are not expected to replace classical computers for everyday tasks. Instead, they will be used for specialized high-level tasks that require capabilities that only quantum computers have. Quantum computers and hardware implementations of quantum computers, known as quantum processors, exploit concepts and principles of quantum mechanics. Yet several companies and research institutions are already exploring hybrid solutions that allow for different implementations. And even though quantum beyond-superposition and entanglement characteristics offer advantages concerning quantum parallelism and quantum complexity classes, they also produce a variety of challenges in terms of reliability, error-correction, connectivity, topological protection, and other factors. For especially within a decade, quantum computers will have developed more specific applications. They will be so optimized for specific tasks that still will be many orders of magnitude faster and cheaper than classical computers.

Many companies already have developed quantum computers that are available via the cloud. They allow users to simulate quantum computing experiments. The most powerful quantum computer, which works with the quantum annealing algorithm and is

able to solve Markov chain optimization problems, features 5000 qubits. They are used mainly to optimize routing in traffic simulation, scheduling prototype production, improving recommendation engines, and others. Other quantum computers with smaller numbers of qubits are being applied to molecular chemistry problems in quantum simulations, thanks to their appealing capability of representing the Hamiltonian of the molecular system efficiently.

1.6.2. Neuromorphic Computing

There is another area of computing research that is getting significant attention and investment, both from government and military funding agencies and research groups, and industry groups interested in developing useful specialized computing systems, particularly for data analysis and machine learning applications. Neuromorphic computing establishes a mapping of computing environments onto hardware in such a way that the fundamental characteristics of the hardware itself may be harnessed to improve power, efficiency, and speed. Although systems based on neural network ideas and technologies have been developed for decades, as a consequence of practical limitations of the underlying hardware, these systems have become mostly software-based, emulating the functionality of neural networks. Neuromorphic computing seeks to recast those neural network environments onto specific hardware devices which are representative of the characteristics of real biological neural networks. These devices do not require an emulatory environment in software. They are designed to use digital or analog components to create integrated circuits that mimic the functionality of real neural networks.

The advent of commercial fabrication capabilities that enable prototyping of specialized neuromorphic processors for specific applications is enabling an explosion of research into systems that perform particular mapping of traditional neural network-like systems onto neuromorphic chips. These chips may incorporate specialized resistive and memristor components into the modeling of particular aspects of neuromorphic networks. Recent commercial investments in embedded chip computing systems for data analysis have validated the potential for accelerated performance at reduced power and efficiency costs. The advent of architectural level techniques that enable mixed digital-analog processing as a complement to classical digital processing for a subset of data-intensive applications has fueled investments into neuromorphic computing systems that target reduced cost positional systems. Nanoelectronics are enabling fabrication of devices with the memory and processing elements integrated into a single transistor architecture to create power and area efficient implementations of intelligent systems.

1.6.3. Flexible and Wearable Electronics

Flexible and wearable electronics present new design challenges. Low-cost and high-volume manufacturing of functional electronic devices on flexible substrates is an attractive proposition for many applications. The push towards flexible and wearable electronics has led to the adoption of new fabrication and processing technologies that are less evolved compared to traditional silicon technologies, rely on different device architectures and materials such as oxides and organic semiconductors, and target different application paradigms. However, the progress that has already been made shows that flexible and wearable electronics is a realizable proposition, waiting to be fully realized. The research work done to date has targeted various aspects of flexible electronics, and widespread implementation of these technologies is expected to occur in the near future.

Flexible displays and organic light-emitting diodes driven by transistors fabricated on plastic or polymer substrates are already commercial electronic products. Organic and flexible amorphous silicon circuits are being developed that target novel applications such as low-cost active-matrix backplanes for devices, electrophoretic displays for e-readers, and sensors on curved surfaces. Organic sensing systems fabricated on flexible organic transistor-driven circuits have been demonstrated, targeting applications such as the human cardiovascular system and environmental sensor networks. Other highlights include triboelectric power sources fabricated for thin-film energy harvesting, OLEDs integrated with organic light-sensing devices or organic solar cells to develop conformable and phototropic devices, fully integrated low-power wireless communication and integrated circuits integrated with flexible batteries, and integrated circuits integrated with driven RF switches for flexible radio-frequency applications. Wearable electronics, which are a subset of flexible electronics, are expected to further impact human healthcare, military, sports, and other domains.

1.7. Conclusion

The trajectory of VLSI circuit design has undergone a radical change in just over a decade, and while the trends began at first as minor ancillary developments serving to meet the requirements imposed by density and scalability, they have rapidly become core approaches and driving forces behind the majority of important recent advances. Indeed, hardware design is now continuously pursued in synergy with algorithmic design at all levels of abstraction. The thrust-to-density ratio which has characterized the history of circuit design during the Moore's Law era is being transformed into a multiparameter optimization that seeks to minimize energy, latency, area, and design time, while maximizing bandwidth and yield. Algorithms are moving to the forefront, as problems long thought to be intractable due to their sensitivity to noise and other nondeterministic

effects, or their expensiveness due to searching for the correct solution from the space of candidate solutions, are being addressed through innovative hardware-assisted solutions based on both reconfigurable, specialized integrated circuits and application-specific VLSI. Hence, we are witnessing a democratization of the IC design process, with a concomitant acceleration of exploration into new application domains and VLSI architectures in benevolent exploitation of the Moore effect.

Will this trend continue to the point where design systems will autonomously invent innovative solutions for ill-defined user problem statements? Certainly, some incremental progress in this direction can be expected through ever-increasing sophistication in system modeling techniques and back-end implementation capabilities. Perhaps more to the point are some analogies with earlier radical shifts in circuit design practice which followed major technology revolutions that ushered in new design ecosystems. We discuss this possibility in the next section, considered by some to be the central theme and message: While it is tempting to adopt the minimalist agenda of meager incrementalism against a varied backdrop of much intellectual activity, history would appear to suggest that more substantive paradigm shifts in the near future years or decades would not be out of the question.

References

M. Zhang and R. Patel, "A Hybrid Neural-RF Model for Next-Gen Wireless Communication," IEEE Trans. Commun., vol. 71, no. 2, pp. 456–467, Feb. 2025.

L. Hernandez et al., "Low-Power SoC Design for Edge AI Applications in 6G Networks," IEEE J. Solid-State Circuits, vol. 60, no. 3, pp. 512–523, Mar. 2025.

J. Kim and S. Rao, "Smart CMOS Amplifier Architectures for Adaptive Wireless Interfaces," IEEE Trans. Circuits Syst. I, vol. 72, no. 1, pp. 88–99, Jan. 2025.

Y. Li and K. Singh, "Reconfigurable Baseband Processing for 6G Smart Antennas," IEEE Access, vol. 13, pp. 12345–12356, 2025.

A. Das and B. Kumar, "Deep-Learning Enabled Modulation Recognition in IoT Devices," IEEE Internet Things J., vol. 12, no. 4, pp. 2001–2012, Apr. 2025.