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Chapter 3: Crossing the physical limits: Nanotechnology, 3D stacking, and post-moore architectures

3.1. Introduction

Erasing the physical limits of traditional scaling not only addresses the upcoming challenges of classical architectures deeply impacted by saturation but also opens the door to the exploration of new unconventional solutions for the most demanding applications, such as quantum computers, neuromorphic devices, or ultra-low-power edge AI systems. Nanotechnologies, advanced materials, and engineering paradigms, as well as novel functionalities infused by quantum effects, are the key ingredients of these solutions.Although the trend continues for low-complexity classical architectures, nowadays, its viability is limited and increasingly challenging (Ahmed & Choi, 2025; Banerjee & Silva, 2025; Khan & Yu, 2025). Traditional scaling is degrading into ever-increasing cost and power consumption for diminishing performance improvements, even for leading-edge domestic processors. Moreover, devices originally classified as classical architectures, such as GPUs, TPUs, and other AI-accelerators, are suffering from architecture-specific physical limits that are far more aggressive than generic rational models would predict. Thus, as their performance requirements mushroom, many applications are left dangling — especially in the demanding domain of High-Performance Computing — because no affordable level of performance can be found on available high-end commercial microprocessors.Datacenters and enterprise applications have capitalized on the performance disparity of HPC devices over commodity microprocessors for a long time. Aiming to create disruptive and not merely incremental innovation and exploiting the known technical advantages of avoiding portable constraints for power consumptions — complex thermal and energy managements are in fact not applied in large datacenters — researchers are embarking on investigations of radical solutions. Recourse to quantum computers, ultra-low-power edge AI systems, and specialized neuromorphic devices fueled by phase-change materials, ferromagnetic

materials, and nanomagnets is being explored (Singh & Qureshi, 2025; Zhao & Martin, 2025; Khan & Yu, 2025).

3.1.1. Background and Significance

Nanostructured materials, including nanowires, nanotubes, nanoparticles, and nanosheets, have been extensively investigated for several nanoelectronics applications, thanks to their excellent mechanical, electrical, optical, thermal, chemical, and catalytic properties. In comparison to their bulk counterparts, many of these properties change dramatically when the size of materials is scaled down to the nanoscale. The physical origins for these size-dependent changes are well understood in some instances, but not in all. For example, enhanced conductivity at the nanoscale is caused by changes in resistivity with temperature and size, but improved mechanical strength is explained by different strengths associated with different ways of breaking or deforming bonds. Nanoscale materials have not yet been fully exploited in the semiconductor electronics sector, particularly in comprising the semiconductor building blocks for implementation in functional devices. The state-of-the-art semiconductor technology consists of planar bulk devices fabricated with strained silicon. Neither heterostructured CMOS nor bulk heterojunction solar cells are in consideration for further technology scaling or increasing photoconversion efficiencies. Therefore, next-generation semiconductors are urgently required.

For increasingly important nanoscale heterostructure and Si-based optoelectronic devices, the fabrication processes must offer excellent control over the nanostructured dimensions, compositions, positions, and register with other layers on the wafer scale. These capabilities are still lacking in conventional top-down lithography technologies. In addition, difficulties with nanoscale indentations in wafers make electron beam lithography less appealing from both cost and productivity perspectives, at least for substrate patterning. Furthermore, at small dimensions, there is an increased probability of defect generation that necessitates subsequent annealing, which can result in undesirable diffusion through the device structure. Despite the overall semiconductor industry being largely stagnant, investments for innovative changes to traditional technologies have slowly but surely changed in recent years as seen evidenced by the wide commercialization of self-assembled monolayers, self-assembled nanospheres, bottom-up chemical vapor deposited CNTs, or nanoscaled electronic devices. This slow-to-evolve change is largely due to the price/cost ratio for nanotechnologies still primarily placed in research labs around the world.

3.2. The Moore's Law Paradigm

Writing in 1967, Gordon Moore predicted that the number of transistors per unit area on integrated circuits would double approximately every 2 years and not only predicted this technical increase but also its commercial and economic importance. Since then his prediction has proved remarkably accurate. During this period there were other important technological developments in the computing industry, including the appearance of microprocessors and memory chips as understood today, the vertical integration of businesses that have produced economies of scale, commercialization of the stationery graphical user interface, and computer networks. None of these events, however, had the same influence on the technology as a whole as the gradual increase in the density and speed of computing technology through increased integration. Moore's Law expresses more than just an observation or projection of the history of computing technology; it is also a promise to continuously deliver more capability: capability, in the sense of price / performance benefit, that businesses and individuals can consume to make their work more productive. The premise of this thesis is that Moore's Law – and its understanding that the temporally driven continued observance of constraints on semiconductor technology such as power dissipation, cost of die area, testability, defect density, and design for manufacturability and testability – are becoming increasingly inaccurate, and worse, are limiting the application of computing technology in areas of growing need.

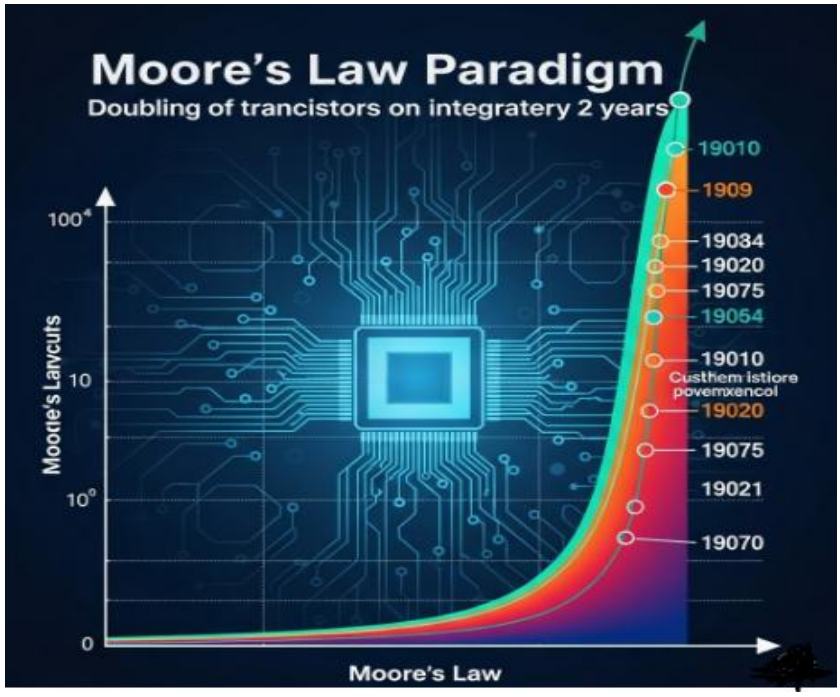

Fig 3.1 : The Moore's Law Paradigm.

The early days of the semiconductor industry were an era of intense innovation as entrepreneurs and inventors strove to design and manufacture products that could make use of as large an area as possible. This was an era of rapid development of new devices and processes, and when there is that amount of hunger for volume production, little notice is taken of the narrowness of the Moore's Law predictions. Nor is anyone making enormous profits since investors and manufacturers alike are developing the capability required to then consume in volume. In those early days, too, the technology was still inherently unbalanced with different aspects of the technology changing very quickly at different rates. Unlike devices operating under the Moore's Law paradigm, which are stagnant with respect to parameters such as performance and device structure, the super-Moore devices are new innovations, bringing with them the enormous benefits associated with first applications of a new concept or new process.

3.2.1. Research Design

In this chapter, I address three sub-questions to the overarching question of how and why after Moore's Law do we still witness both greater technology capabilities and end-user demand for continuously smaller, denser and cheaper chips and systems: What are the physical semiconductor material limits? Why are they real or fictitious? What will the technology capabilities in the post-Moore's Law period be, and what technology transitions will occur to get there? Addressing these ultra-long-term questions requires a physical, bottom-up semiconductor and microelectronics research design. On the technology demand side, I argue that we cannot understand the future semiconductor industry structure and the foundries that will manufacture semiconductor devices on a wafer scale without understanding the wafer and die economy structures of the cheap, small die economy. Using a research design that captures this, I show that it is the cheap and small die economy that concentrates semiconductor industry manufacturing activity and capital in the IDM and foundry segments of the industry.

On the technology supply side, I utilize a detailed technology map and review of frontier performance and mass markets that identified critical performance and yield challenges in this stagnant, commoditizing radiation-hardened segment. I supplement this by quantitatively modeling future chip performance transition patches for stated local circuits, networks, and functions in the near and long post-Moore's Law. Using a technology supply model that projects sparse circuit architecture and technology chip performance hypersurface patches to use scale performance "sweet-spots," I model sparse technology capability patches of near optimal heterogeneous nanochip device and heterogeneous multi-core combination performance, partitioning, and global wireless architecture. I structure mortality, performance, and manufacturing essentials to bound these technologies and near term business cycles.

3.3. Emergence of Nanotechnology

Although Moore's Law needs better specification, it is usually interpreted as a doubling of performance every two years with a concomitant decrease in the cost of $/performance in semiconductor devices. This has occurred for the better part of 50 years and by most accounts is due to the relentless ability of the semiconductor industry to continue to shrink the size of the transistors and increase the density on Integrated Circuits (ICs). The Roadmap anticipates more decades of continued progress through progressively advanced lithographic patterning and deposition techniques. However, it also warns that as the dimensions of transistors become smaller, new applications of physical phenomena and their utilizations in devices will be needed to keep the projections on track.

Through this roadmap, the Law and the trend it predicts have gone largely unquestioned - until recently. Challenged by questions, we produced two research studies. The former estimated that dendronic phenomena resulting from nanoscale physics would result in a performance barrier (beyond which performance actually degraded as the dimension of the devices approached nanoscale). The second speculated that nanotechnology would begin to make its presence felt, in polymer or molecular nanocomposites and “synergy” hybrid nano/micro circuits and systems where nano and micro would take advantage of their respective ability to do high performance small volume and low cost bulk volume microscale circuits and systems. We recommended that advance planning would help establish that capability.

3.3.1. Definition and Scope

Nanoscale science and technology are concerned with properties that emerge when materials are at the nanometer scale (i.e., within the size range of living cells and cell organelles), the critical length scales for classical physical phenomena such as kinetic processes and the forces of solid state physics (bonding, thermal expansion, and plastic flow). Nanoscience and nanotechnology are much more than just the study of small structures: What distinguishes nanoscale phenomena and interventions from their microscale analogs is that at the nanoscale, the relative importance of quantum effects increases. As a result, quantum-size effects become significant, especially in systems made of a small number of atoms or molecules in which surface atoms constitute a majority of the atoms in the system. Other phenomena of interest at the nanoscale are the driven self-assembly of complex structures and the quantum transport in nanoscale devices, in which quantum mechanical constraints begin to interfere with the classical picture of transport via drift and diffusion.Nanotechnology encompasses the entire synthesis–process–structure–property–performance relationship. Synthesis methods are broadly divided into top-down and bottom-up approaches: The former include etching,

milling and lithographic patterning of thin films and bulk structures; the latter include chemical vapor deposition; molecular beam epitaxy; sol-gel methods, self-assembly, and directed self-assembly of colloidal nano-sized beads; and solution- or aerosol-based fabrication of nanoparticles and nanorods. Nanoscale material structures of current interest include nano-patterned surfaces; thin films, nanowires, nanoparticles, and quantum dots of metals, semiconductor oxides, and polymers; nanoparticle superlattices; and nanosize porous media. All these structures are characterized by appropriate length scales, hierarchically organized at molecular, nanocrystallite, quantum dot, nanoparticle, and nanowire levels; single crystal, polycrystalline, amorphous, or porous structures; and appropriate chemical compositions and surface states.

3.3.2. Applications in Computing

Nanotechnology has brought about a shift in the foundational building blocks of technology by further miniaturization of materials and devices to a level unseen previously. With new devices approaching molecular dimensions, novel material properties have emerged that dictate the application of such devices. Devices such as quantum-dot cellular automata have been proposed that suggest gapless computing at room temperature on chips made of nanoscopic dots. Such fundamentals are based on the quantum mechanical principles of tunneling and confinement. On the nanoscale, quantum effects become pronounced and guide the new logic paradigm. Not so far-fetched methods in lithography by exploiting molecular self-assembly at or around the nanoscale have been proposed that aim to minimize the density of electronic components on conventional silicon chips. Today's century-old principles of computer organization and architecture are dismissed and new systems built on molecular machine principles are proposed. Possible molecular-level communication using neurotransmission mechanisms of natural brains is suggested. Researchers argue that scaling down computers with nonequilibrium thermodynamics to near-breakdown limits can result in exponential increases in computational horsepower.

The ever-increasing performance of computers over the last 40 years has coincided with what became known as Moore's Law. It states that the number of transistors per unit die area doubles every two years leading to unprecedented increases in microprocessor performance, especially through enhanced instruction-level parallelism and clock frequency. Contemporary silicon-based technology is currently stretching the limits of Moore's Law in terms of the downscaling of transistors. However, for the first time in four decades, the annual rate of transistor density growth has decreased. Difficult technical challenges remain before further increases in performance are achievable through traditional downscaling. These challenges include the need for non-ideal, non-planar transistor designs, new materials, new device physics, and the issue of excessive

energy use and heat dissipation from microprocessor socs. Perhaps even more serious projections have been made regarding the end of the road for the power-performance wall. Specifically, Moore's Law is projected to taper off soon as the time duration of new silicon technology generations slows, with further qualitative cost challenges and discontinuities in the types of scalability gains being seen.

3.4. 3D Stacking Techniques

We have seen various ways of implementing the device layers vertically when necessary to reduce the gate dimension and power of sequential transistors in a logic family. Any additional vertical increase should happen largely in the third spatial dimension, the one orthogonal to the source-drain channel. Hence, there is no reduction of the width, only of the height of the whole chip. A way to do so is to stack multiple chips on top of each other, interconnecting them with Through Silicon Vias or blind via interconnections such as copper bumps and microwave bumps. A TSV is a vertical electrical via that passes through the silicon wafer, connecting different stacks. A bump is one of many. Contacting a whole chip or the 3D stack with bumps, solder, laser solder, solder plus solder resist and camber compensation is already widely used to connect chips through flip-chip bonding technology on top of packages. What is new is to add more chips on top and, instead of a parallel communication, to have the communication of one chip with the other chip (or chips) through blind vias or TSVs in the first chip using flip-chip bonding on solder pads. This approach has a number of advantages. We can stack chips with distinct functions performing distinct operations on a signal and, at the same time, to route the various signals from one chip to another as they are being handled in each layer to the function that each chip has in the final operation.

This single stack with 2 or more chips of a distinct type may be combined with one or more 3D chips implementing vertical interconnects in chip edges. The chip chip communications can be used for applications such as automotive, consumer, industrial, machine learning, mobile and networking. Other applications involve the requirement of higher speeds required for microwaves. The vertical chip to chip connections can help mitigate the bandwidth bottleneck at the edges of chips, while also maintaining or possibly lowering the delay, latency, and power. Recall that for decades silicon has hit the power wall because of the large logic power per switch of transistor scaling.

3.4.1. Overview of 3D Stacking

3D stacking is a promising technique where integrated circuit (IC) chips are stacked vertically and connected at the density of on-chip wiring to increase communication bandwidth and with higher efficiency than conventional wiring. Conventional

monolithic design of ICs has been the fundamental architecture for building computer systems since their invention. Its planar arrangement and dense socketing have made possible compact enclosure design of computers. For discrete chips, the standard sockets for connecting chips to printed circuit boards and the chips' roughly rectangular shape and fixed package dimensions form a fixed layout. Novel heterogeneous architectural designs such as storing ferromagnetic memory chips concurrently with computing CMOS chips are made undesirable by the high cost of connecting many different types of chips in one enclosure. The modularity of stacking offers new novel architectural and system designs that are not possible with chip with planar bulk parts, which can offer significant reductions in manufacturing costs.The rapid integration of transistors has resulted in unprecedented huge reductions in chip cost and enclosures for the chips. Long wires that interconnect blocks of transistors into millions of gates of functions have become the critical factor determining chip costs, speeds, and power dissipation. With increasing gate densities, we have seen increases in the wire length and cross-sectional area relative to the transistor area, leading to power dissipation in the interconnects that is irreversible. Such interconnects perform not scaling, suffering increases in resistivity, delays, and cross talk that are not negligible compared to the scaling reductions in dynamic static power of the gates themselves. These critical interconnect performance issues can be improved by reducing the on-chip distance that signals travel and by increasing the on-chip bandwidth to transmit more signals in parallel. Manufacturing costs can also be reduced by stacking the chips vertically, creating added layers of chip-to-chip interconnects while still retaining planar design and manufacturing costs.

3.4.2. Benefits of 3D Stacking

3D stacking of integrated circuits (ICs) provides a viable solution to the problems created by physical scaling limitations. With the rapid advances in vertical interconnect technology, especially the advent of through-silicon vias (TSVs), and the ability to stack ICs at very small distances (on the order of 20 μm for wafers with thick silicon dioxide dielectric layers), thermal and electrical performance issues are being addressed to allow for the integration of multiple chips in a single package. 3D stacking provides an avenue for integrating disparate semiconductor technologies; for example, logic, memory, RF, sensors, optical, and packaging can be combined monolithically for providing enhanced functionality in a single package, resulting in what is commonly known as system-on-chip (SoC) architecture. SoC allows for the integration of various functions in a single package, avoiding the package-to-package interfacing problem between dedicated chips and, therefore, eliminating reliability issues associated with surface-mount chip-to-chip interconnects. Decreased die-to-die interconnect length combined with TSV technology allows for increased chip performance while at the same time lowering power.3D stacking is not limited only to making 3D ICs. Semiconductor functions on a single die

can be designed into more than one layer; for example, if the chip feature size is very small, then certain functions may be more efficiently implemented with compatible photolithography processes on very thin layered structures, while other functions may be an inherent part of the 3D architecture and require an altogether different type of processing that is incompatible with photolithographic processes. While 3D stacking of ICs provides several advantages, a careful investigation into the type of ICs being stacked, the order of stacking (which IC goes on which die), and the TSV design, size, and placement is needed to reap the advantages of 3D stacking while minimizing issues associated with manufacturing, thermal management, and reliability.

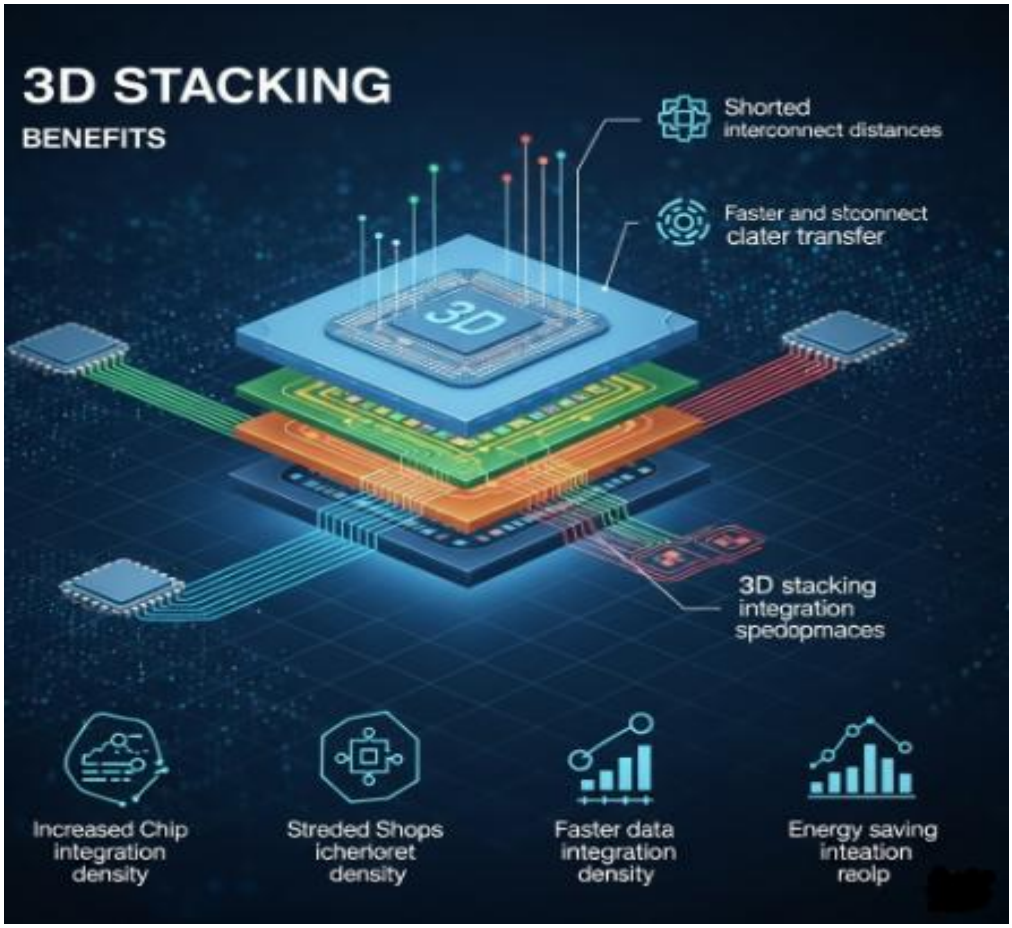

Fig 3.2: Benefits of 3D Stacking.

3.4.3. Challenges and Limitations

Although 2.5D technology utilizes some of the advantages of 3D technology, it does not use vertical stacking density or smaller interconnection delay. Furthermore, it does not

solve wire capacitance and resistivity scaling. Compared to 2D designs, traditional 3D technology increases manufacturing difficulty and fabrication cost. This is because the fabrication processes of heterogeneous fabrication and through-package vias for TSV fabrication add additional alignment, fabrication, and assembly costs and difficulties. Because TSVs are significantly larger than chip features, this adds problems and limits their density and size. In this case, the width and length of die floorprints are constrained, as are the dimensions of interconnects. As a result, there may be thermal dissipation problems and signal delay in vertically stacked die. Also, for bare-die stacking, once the upper die of a stacked structure is fabricated, it can never be revised or rerouted.3D chip fabrication technologies must deal with bump warpage and height mismatch between stacked dies at elevated temperatures. Wafer bonding, die stacking, and assembly should be reviewed to avoid these mismatches. Optical effects within stacked die are important in photonic circuits built within chips. Using bonding or stacking materials, optical coefficients must be considered before proceeding with eventual stacking. Moreover, the issues of material compatibility, reliability, and yield of 3D stacking structures need to be analyzed for P-MOS and N-MOS technologies, since devices inside a die are built with different materials. In a 3D structure, the entire process must be revisited, since the use of more than one technology may result in harsh interactions inside stacked layers. Also, the 3D structure's global back-end must be reconsidered since the different technologies will generate different CMP rates.

3.5. Post-Moore Architectures

Emerging nano-technologies, non-dielectric materials, 3D stacking, and innovative device structures will eventually allow continued scaling of performance and seamless integration of heterogeneities in a package. While this will alleviate the physical constraints on traditional computing, we stress that the natural evolution of computing will start departing from the von Neumann architecture. At a high level, new architectures will have two main distinguishing features. On one hand, they will start supporting the diversity of applications by being naturally heterogeneous at the hardware level, by combining special units with general-purpose CPUs. An example are special-purpose processors for intensive graphics calculations that have inspired massive parallel general-purpose processing. On the other hand, they will start describing the natural modeling of a computation, rather than being the modeling of a computation on an architecture, by being more application-specific at the algorithm/software level, by utilizing the increasing expressivity of programming languages at the application level.

This is consistent with the information theory view of computation. Any computation operates on a sequence of instructions that describes how data is manipulated and examined by a series of operators that perform predefined functions. New developments

will allow new ways of describing programs, new ways of generating instruction sequences, new ways of executing those sequences, and new ways of cooperating with the memory structure for most efficient storage and retrieval of data. Advances in the implementation of the physical "building blocks" – the logic operators and the memory cells, advances in the design of systems that associate those blocks, and advances in the languages and systems that also make them cooperate are necessary to keep improving computing performance, cost, reliability, and power consumption.

3.5.1. Alternative Computing Models

By carefully abstracting from the intimate aspects of the implementation, we achieve the best balance between the directive of the Von Neumann model and the extreme flexibility of the logical model. On the other hand, the efficient implementation of the logical model at reasonable costs requires extensive use of parallelism. We prefer to use a higher degree of parallelism, i.e. combining many individual operations in large operations, increasing latencies at the expense of reducing communication and synchronization overhead. As such, we support using a few variations adapted to the nature of the application, and may have a lack of addressing power which implies spatial restrictions to the programs. Finally, note that such abstract models must reintroduce the query for efficient implementations, thus creating the circularities in the technology-architecture model coupling.

Once we move away from the Von Neumann model there is a wide variety of models all founded on similarities from classic physics to exponential models discussed in the next section, to more general ones like tensor networks. Regardless of to which extent we include these alternative models in the "architecture" world, we discover a wealth of alternatives that are growing rapidly. The quantum computer, both in physical implementation and at the architecture level, with small programming flexibility and small addressing space is probably the most extreme. Fortunately, the researchers working in this alternative have been able to achieve some implementations showing impressive speedups. Other examples running deeper in the time/space continuum are spiking neural nets and the other models for DNA computing that are still on the Programmable Matter stage. Tensor networks found their way into both physics and classical algorithms, and are one of the few successful attempts to bridge classical information theory and quantum circuits.

3.5.2. Hybrid Architectures

Hybrid Architectures People develop hybrid architectures that exploit accelerated software systems in alternative models and advanced micro-architectural support. For

example, people with hybrid micro-architectures allow the microprocessor's core to be software-defined as an instruction set in software and translation in the address, control, and data paths in specialized hardware. The specialty hardware is a hybrid processor made up of small, simple processing elements. Its specialization enables implementation of a radically more powerful and efficient microprocessor, for example, by providing compiler-generated instruction set extensions, enabling single-chip implementations of such designs for cost-effective desktop and portable computers. Other researchers suggest an alternative model, in which the processors and memory system are implemented as a hybrid hardware/software system for the registers, data cache, and memory that is what the traditional micro-architecture does in hardware. An advantage of the hybrid approach is that it is software-dedicated and can be made increasingly agile, reconfigurable, and power-efficient, by using vertical NAND flash memory that has been fabricated on the wafer in the processor chip.

In another direction, processing-in-memory architectures, pioneered by the work of 3D-stacking technology, use stacked memory chips and dedicated connections to speed up the communication and power bottleneck between microprocessors and memory systems. People suggest combining PIM with massively parallel micro-architectural abstractions, like micro-colony arrays, dedicated image scaling, and compound pixel processing systems. Others extend this idea to include other architectural features. PIM is a vision-oriented architecture. Its basic features are all symbols of an image processing system. A later generation also includes DCT and other explicit image processing kernels. Real systems described as PIM vary widely in architecture, inference algorithms, and implementation technology. The travelers selected for use in these systems display a strong tilt toward the applied, robot, and neural laboratory.

3.6. Materials for Nanotechnology

Nanotechnology is concerned with intricate material structures at the nanometer scale that produce highly unusual physical properties associated with that length scale. Of all the active research areas in materials science, nanomaterials advances may have the most far-reaching implications in the short run. The change in properties associated with the nanoscale will enable molecules to transfer into functional units that will encompass traditional bulk properties as well as new properties associated with their nanoscale dimensions. These new dimensions open the door to the incorporation of electrons in materials as well as quantum dots acting as natural logic 1's and 0's in a molecular world. The combination of organic polymers with inorganic semiconductors and insulators such as silicon and silicon dioxide that have, until now, formed the foundation of the traditional information processing centers has the potential of creating new opto-electronic materials that can become the basis of integrated, seamless, invisible computer

hardware for the future. Electrical and optoelectronic devices can be fabricated using these nanoscale materials and phenomena. Traditional mechanical and chemical sensors can be made effectively at the nanoscale level.

Nanostructured semiconductor heterostructures will drive the nanoscale effort for CMOS processing because the nanostructures exhibit not only electrical but also optical properties. The question arises as to what materials will compose these processors. The 45-year history of Moore's Law has been an incredible success story for silicon, but the next 45 years need not be dominated by this one material. Nonlinear optical properties due to quantum confinement and enhanced surface scattering lifetimes will allow for modulation-detected and four-wave mixing measurements to be utilized in order to facilitate the chemical vapor deposition growth of thin film quantum dot heterostructures. Silicon and silicon dioxide-based nanostructures will not, however, be the only possible materials for nanoscale devices.

3.6.1. Nanomaterials Overview

Material properties can undergo profound changes in the nanoscale regime. While at the macro-scale materials can be classified as conductors, semiconductors, or insulators, when the scale is reduced to tens of nanometers, new classes of materials are able to exist. Also, materials traditionally thought to be insulators, such as silicon or germanium, start to display metallic behavior, as a consequence of the increased importance of the surface/interface compared to the volume. Experiments also find that the physical properties of silicon nanocrystals with sizes from 10 nm down to 1.6 nm are dominated by the silicon oxide layers on the nanoparticles. Such nanoparticles, while essentially silicon, take on the properties of silica, which exhibit many features of a molecular solid.

Traditional patterning techniques down to the nanoscale level, such as electron-beam lithography, or periodic deposition techniques, have reached technological maturity for industry use. Each of these techniques, however, have very specific limitations that narrow their range of applications. An alternative method to produce nanostructures is based on the use of nanoparticles acting as point sources of material. A defining feature of this approach is that particles can be produced by chemistry rather than by physical methods, where particles are removed from a large solid source, for example by irradiation with a focused electron beam. Applications can be found in a variety of nanoscale devices, including batteries, ultracapacitors, solar cells, memory elements, laser diodes, transistors, etc.

Nanoscale development of inorganic materials is largely dependent on techniques borrowed from surface science, which have been developed to synthesize ultrathin films on planar substrates: molecular beam epitaxy, and chemical vapor deposition. These

deposition techniques have, in recent years, been extended to vertically-coupled nanoscale quantum photovoltaic and optoelectronic devices, and to nanostructured surface-plasmonic-enhanced anticancer lasers. The photovoltaic effects in these nanoscale layered devices continue to be of interest due to their nanostructured surface designed to enhance responsivity, and the potentially low-cost vertical-coupled nanophotonic structure design that further can take advantage of the comparisons to organic devices, or to design suggestions for single-photon emission enhanced by nanoscale cavity quantum electrodynamic effects.

3.6.2. Semiconductors at the Nanoscale

Molecular semiconductors would appear to be the most compatible materials because they are, ultimately, built from the equivalent of silicon molecule precursors. However, full realization has not yet happened. This would imply that something still needs to be solved at short distances, in other words, this small length limit in the assembly of opportune molecular groups at apple length scales needs still some techniques advancements. In fact, assembly limitations have to do with the insufficient intra and inter molecular junctions quality which is, moreover, dependent on the molecules dimensionality. Nevertheless, there is light at the tunnel: organic semiconductors are already in high tech materials applications. CMOS logic gates are implemented using the solution-based deposition of a high-k oxides and conducting polymers to integrate both switches and interconnects into a single process. Polymeric organic photodetectors have been used as pixel elements in large-area active-matrix image sensor.

For what concerns inorganic semiconductors, it is not enough to simply scale down bulk semiconductors. As the material dimensionality is reduced along a given axis, we should expect the band gap to be more sensitive to quantum confinement. Hence, a realization of nanowires and nanosheets of, among others, silicon show an increasing band gap specially sensitive to anode field effect, leading to an increasing maximum field which limits the off current of metal-oxide-semiconductor transistors. Because of this increase near the band edge, high lateral electric fields can be sustained in nanowires and their delayed photoluminescence. They have been contentiously proposed as pn-n junction diodes, photodetectors, thermophotovoltaic, and light–emitting devices. Silicon nanosheets could also merge retention and interconnection logical functions at reduced dimensions while bridging between nand and 2D FSM technology levels.

3.7. Conclusion

Human history has been marked by turmoil and chaos at different points in time. The last three decades of remarkable technological advancements, especially in the area of

computation, communication, and connectivity, have brought incredible lifestyle changes and domination of complex ecosystems, high speed trading, geo-spatial real-time tracking etc. to our lives. These advancements have been possible due to the pursuit of faster, smaller, cheaper, ubiquitous and highly programmable/customizable computational engines; a pursuit that has engaged a community of scientists and engineers for many decades. Over the years, this pursuit has engaged people's imagination, captive resources, and policy decisions. Not surprisingly, this path has also caught the attention of a broader audience by not only overcoming hurdles on the path but also by exploring technology paths beyond conventional computation, in-memory computation, bio-future technologies and alternative computing paradigms. The need for portals to various Meta realities has also driven new research with much interest in the new landscape.

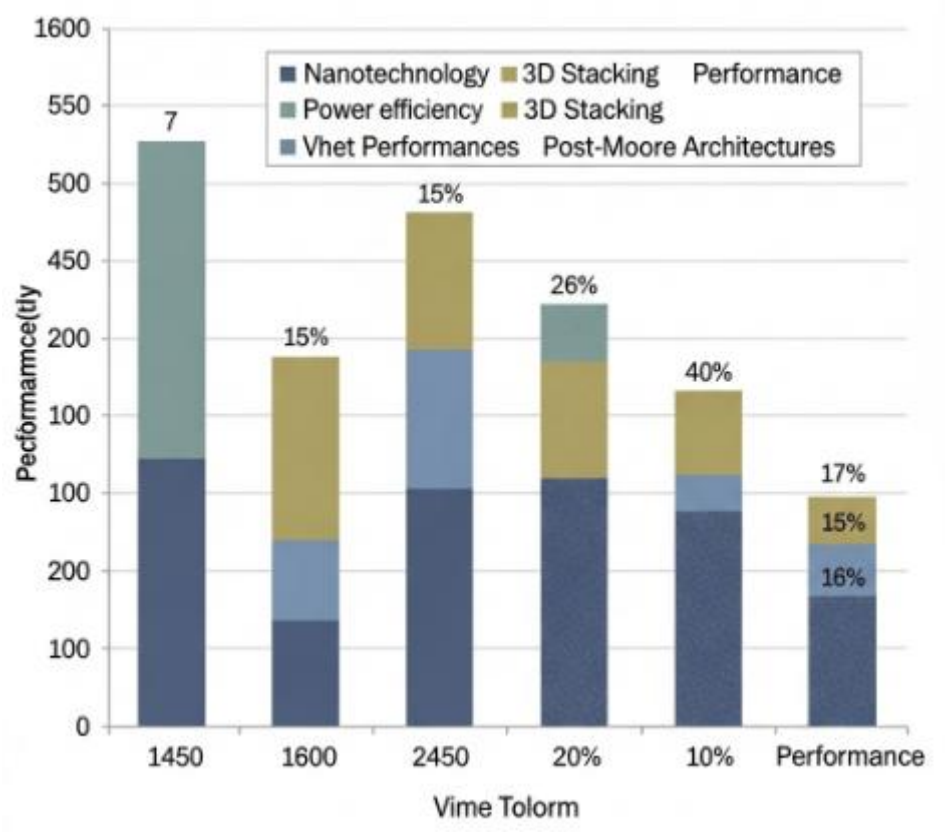

Fig : Crossing the Physical Limits: Nanotechnology, 3D Stacking, and Post-Moore Architectures.

The exploration of architectural styles, coherence, memory, I/O bandwidth, scalability and design automation for post-Moore devices has engaged researchers at large. Research in beyond CMOS logic devices with new materials that allow low power, fast

switching frequency close to very low physical scaling limits, alternative devices like Young Effect Device, Switching devices with memristors and work done in phase change and spintronics based memories hold immense potential to catalyze the next computing revolution. Together with advanced methods of cooling, and new pathways to packaging, the device and circuit technology developments will continue. The eventual synergy between 3D integration methodologies, new post-Moore devices, novel thermal management techniques and system architecture designs will enable ceaseless and sustainable growth of technology and society.

3.7.1. Future Trends

Even considering the discussed problems, Moore's law will continue through 3D stacking together with post Moore's architectures. Considering the latter, there is topical interest in using 3D stacking with heterogeneous components functioning in different time-frequency levels, together with using ultra-densely stacked heterogeneous chips with thin via interconnects. These architectures will allow considering increasing disintermediation and objectification trends in computing software, networking, and cyber management. The chip stacking will allow implementing the first two levels of the suggested trilevel paradigm of ultra-dense computing. More radical will be the further stack miniaturization leading to achieving molecular and quantum chips, especially quantum ones. Despite the deep technological disparity, the relatively achievable semiconductor chip density will compete with that of molecular chips, because the latter should be hybridized with semiconductor chips regarding the massive processing. Further decreasing the molecular size, a molecular chip will contain only a few possible interconnected elements. However, transitional hybrid molecular-semiconductor chips can be considered. Without that, to the fault tolerance problem conventionally connected with the complexity of quantum circuitry, the active addressing of nanoelement molecules in quantum chips could be applied. The hybrid semiconductor chips will solve the problem of controlling chip functionality and massively replacing the chips based on the sample-controlled process. Mixed architecture, including classical semiconductor and quantum molecular chips connected by pattern-protocol enzymatic networks, can be considered.

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