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Chapter 6: Energy-efficient circuit architectures and sustainable power management systems

6.1. Introduction to Energy Efficiency

Energy or power consumption is one of the key issues in VLSI design. The issues of energy or power are so crucial that they alone can, at times, determine what can be implemented. Developing a product that consumes power is certainly not sustainable! The total power consumed by a VLSI circuit is supplied by a voltage source and is given by the product of the digital circuit switching voltage V and the total circuit current I drawn from the power supply. Thus, reducing power consumption in VLSI circuits can be achieved by lowering either the current or the voltage at a constant temperature. It is also feasible and scientifically sensible to exponentially relate the power consumption of digital circuits to the magnitude of the supply voltage V which is raised to the square Jain & Ong, 2025; Mikhailov & Hassan, 2025; Park & Fernandez, 2025).

For addressing the effects of this concept of energy and energy-related parameters, without losing sight of the overriding issues of reducing physical cost and chip area in chip design, it is best to present a chain of interrelated factors and parameters. Realization of the design and its physical implementation must finally relate back to the area of the chip and its cost, and perhaps indirectly to the subthreshold leakage as a consequence of temperature. As specified earlier, the described parameters and interrelationship indeed help in determining the cost of energy and turning circuits into truly smart power management systems, akin to the growth of the concept of Smart Heath.The realization criteria based on the very many factors as outlined call for ways to guide the designer to achieve the desired artifacts. Flowcharts in broad strokes, in usage can indeed provide a rapid no-nonsense guide even in apparently more esoteric areas like quantum effects and novel technologies that may still not have experienced wide-ranging acceptance (Torres & Li, 2025; Uddin & Zhang, 2025; Park & Fernandez, 2025).

6.1.1. Background and Significance

Energy-efficient circuit design practices have been critical for the success of semiconductor technology, allowing billions of low-cost chips to be used in small electronic devices with long battery life. Energy-efficient circuit design is even more important now with the emergence of mobile, handheld devices operating on battery power and connected wirelessly to power-hungry content. The spectacular growth of the wireless Internet and the boom of the new computing paradigm have resulted in an astonishing increase in the demand for data centers powered by electricity-hungry server computers for the purpose of executing heavy and power-hungry applications. Energy has replaced area and speed as the primary design constraint for all systems, and energy efficiency has become the new goal that the entire research community is pursuing.

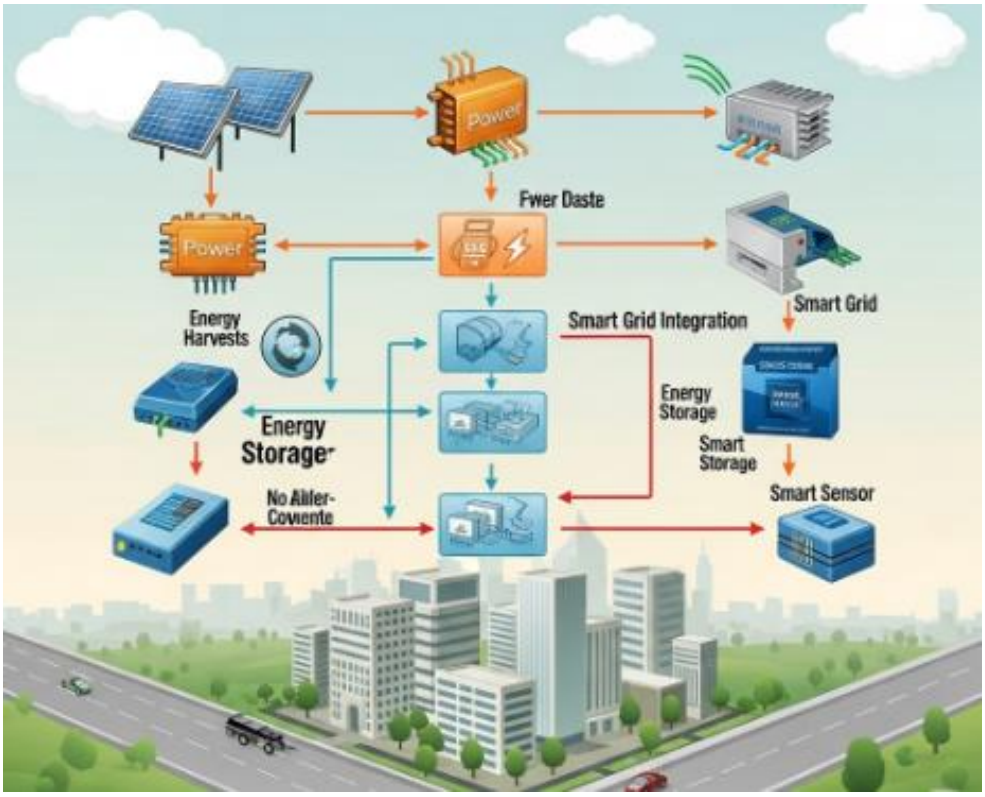

Fig 6.1 : Energy-Efficient Circuit Architectures and Sustainable Power Management Systems.

Power, or more generally, energy has always played a key role in circuit design. The shrinking supply and increasing demand for energy, and the adverse impact of energy generation and consumption on the environment, have made energy efficiency and sustainable power delivery for computational systems a global priority.

In going micro and nano, from silicon to advanced dielectrics or to organic polymers, and from vertical to lateral integration, both designers and manufacturers of systems and circuits have gained a fresh view of the energy-efficiency problem, its complexity and importance, and are addressing the problem from a new approach, focusing not only on the different components of energy consumption in chips, but also on the architecture as well as on the technology for energy-efficient design of integrated circuit systems. In this chapter, we will review only the architecture and circuit level techniques for energy-efficient design of chip systems, while leaving out the material and technological aspects.

6.2. Overview of Circuit Architectures

Energy efficiency is one of the major design specifications for hardware implementation of the computing, sensing, signal processing, and data transfer operations. Efficient VLSI circuit architecture plays an important role in the energy efficiency of the systems. In the past years, significant research efforts have devoted to integrate energy-efficient circuit architectures for various applications such as deep learning, edge computing, data communication, etc. Recently, hardware acceleration emerged as an important keyword for modern computing technology. Specialized accelerator circuits are highly adapted to their specific application principles and they can achieve very high energy efficiency compared to conventional circuits based on general-purpose microprocessors. This section discusses several circuit architectures with a focus on special circuit architectures used for hardware accelerators integrated in applications. Various circuit topologies exist in different levels of the abstraction hierarchy, from device to circuit, to architecture. The overarching goal of circuit design is to realize the desired system functionality while adhering to secondary objectives such as reduced area or power and increased speed or reliability. These parameters are often conflicting; e.g., meeting a critical timing constraint necessitates excessive power consumption or area overhead. Commercially available circuit synthesis tools relax the complexity and time involved in the design process, yet a design engineer must still make decisions relative to aspects of circuit design, such as how to best utilize the available devices; how to best distribute circuit signals over the devices; whether to design for speed, area, power, or reliability; and, if so, how to balance among those conflicting objectives.

6.2.1. Digital Circuit Design

Digital circuits today consist of logic gates such as AND, OR, XOR, etc., flip-flops and latches. Performance characteristics of discrete digital logic gates are delay, dynamic energy, static energy, leakage energy, noise margin, input capacitance and possibly

others based on the applications. These gates are cascaded to create more complex circuits for applications modulated as single function blocks or general purpose processors based on the area, power, reliability and performance requirements. Typically, these applications have application specific characteristics requiring specific design strategies.

Delays in digital circuits are intervals between transitions in logic gates. Due to the switching nature of digital circuits, most of the energy cost comes during the transition phase. The primary circuit delay sources can be summarized as switch capacitance, transition time and logic activity. Delay optimization in digital designs, particularly final stage node driven timing optimization uses slew based driver sizing. Delay optimized cell sets in the required library technology can also reduce performance impact by having transistor sizes appropriate to the delay requirements. Dynamic energy consumption by delay optimized circuits using normal digital logic activity input patterns is controlled by drive strength, load capacitance and input switching frequency.

Other than input patterns, input patterns for multi input gates have a considerable impact on energy consumption and it was shown that low energy pattern dependent library delay optimized cells can give considerable dynamic energy savings. Static energy consumption of digital circuits can come from short circuit, punch-through, sub-threshold leakage, gate-oxide tunneling, gate and junction leakage sources. Typically, we will focus for dense digital circuits, sub-threshold leakage, gate-oxide tunneling components for deep scaled devices. In a nanometer scaling regime, the leakage energy during idle periods can become comparable to dynamic energy during active periods. Hence, in deep scale digital circuit designs, consideration for static and dynamic energy becomes necessary.

6.2.2. Analog Circuit Design

Analog circuit design, with its inherent methodological complexity, is characterized by an absence of straightforward design rules. The conventional approach, utilizing cascading stages, assumes adequate linearity, isolation, and slew-rate performance of each section, thereby permitting overly simplified interstage loading conditions. Guidance in voltage and current levels within components and stages is the only available handrail in the design procedure. Moreover, considerable creative abilities are needed to reach low-voltage, low-power, small-dimension, good-yielding solutions. Consequently, every block requires, to a variable extent, a unique approach that departs from established practices. This is the reason why close collaboration between circuit design, system, and application engineers is essential. The subdivision of the basic functional building blocks for high-performance analog processing is composed of amplifiers, filters, multiplexers, and digital-to-analogs and analog-to-digital converters.

Amplifiers perform continuous, gain-controlled analog signal processing, insensitive to small in-band strength and phase differences of the input voltage or current signals. They address applications such as front-end amplification for RF/telemetry links, filtering and amplification of audio signals, and analog speech synthesis. The pertinent unknowns are noise characteristics, frequency response, gain per section or block, input and output impedance, power supply rejection, distortion performance, and the temporal behavior of output current and power. These characteristics define a demanding multivariable problem. It becomes exacerbated by the attempt to achieve the lowest possible dimensions, power supply voltage, and dissipated power while relaxing the constraints in terms of connecting circuitry and roughening the operating conditions.

6.2.3. Mixed-Signal Circuit Design

When designing mixed-signal circuits, it is important to consider whether power management is done in the analog or digital domain. A key digital circuit design issue is how to deal with fast signal transients which may flow through the digital circuits during re-configuration or when power management mechanisms detect some local electrical anomaly. Suppose that such transients happen because circuit blocks, sensing the electrical anomaly in their power supply circuit, try to switch their states at the same MOMENT, and that current demand during state-switching is relatively fast. This causes a considerable voltage droop, potentially affecting all the circuit paths in the corresponding domain. The fast signal transients may occur not only during state-switching or switch-overs from one operating mode to a different one, but also during the momentary execution of internal logic functions, which drive the output signals to be at a logical state change. In such a case, transients carry a lower bandwidth, but last longer.

The effect of the fast signal transients is that the timing of all the transitions is pin-pointed at the same MOMENT. Fast voltage changes can cause the output signals to have significantly reduced drive capability or to suffer from logic fault effects. Circuit operations conflicting with the protocol have huge design consequences. One problem with the behavioral description of mixed-signal circuits is that, when the analog and digital parts are treated separately, the analog part can assume that the digital part, with its relatively few signal transitions, acts in an unchanging or quasi-static manner. This assumption is only partially correct when we consider important corner cases. Mixed-signal circuit designers have to be aware of the fact that internal digital states may influence the behavior of the analog parts.

6.3. Key Principles of Energy Efficiency

Reducing the power consumption of integrated circuits and associated systems in order to maximize battery lifetime is paramount to the success of most electronic systems. Thus it is no surprise that companies and academic institutions are investing considerable time and energy into optimizing circuits for lower power. In order to understand how low power operation can be accomplished, hosts of ultra-low power, low voltage and energy-efficient circuit design techniques have been proposed and implemented. This chapter is a concise collection of several of the key techniques and practices that are commonly used in various stages of the design process of low power circuits and systems. It consists of simple applications of low power design principles to state-of-the-art cellular modem, video encoder, application specific processor, programmable hardware, microcontroller, and switch mode power converter, which highlight some important design considerations and techniques. Hopefully this chapter might serve as a tutorial for design engineers and students who need to grapple with systems, circuits and architectures which are power constrained.

The need for low power operation has resulted in the investigation of several smart power concepts. Although many concepts fall under the classification of low power, reducing the battery energy consumed is the singular factor that determines the lifetime of energy extracting systems and hence our focus is on developing techniques that minimize the battery energy consumed. The following sections describe what we believe are some important or key low power architectural and circuit design principles and methods followed by smart power management techniques. The methods described are simple, but they have shown to be effective in implementing low energy systems and circuits. This chapter presents both a top-down and bottom-up approach to address the problem of energy consumption at the system and circuit levels.

6.3.1. Power Consumption Metrics

This section deals with the circuit-level power consumption metrics, as they essentially determine the characteristics of the ITD. The short-term average power consumption is normally easier to relate to the printed circuit board (PCB)-based products and system life tests. The number of columns, and column height, and hence the number of bits switched during a non-linear scan across pixels primarily determines the short-term average power consumption for an imaging sensor. The characteristics might lead to saturation of the column outputs for high input light levels during the read cycle. The pulse sequence would therefore experience high-profile gain, leading to large DC signals at the outputs.

The average power metric does not consider duty cycle and is hence less relevant for sensor-based systems with short scan times across sub-arrays of the entire pixel array. Pulse signal waveshape at the amplifier input is from flashing LEDs for indoor use. The input signals are alternated at the Nyquist frequency between odd and even columns for LED-based sensing applications. Switching to optical fiber-based input from the outside world for both indoor and outdoor sensing with very bright input signals would lead to very different sensor power metrics.

The restoration of profiles with non-digital characteristics at the amplifier outputs, and the variation of with input light intensity, therefore lead to saturation at the front ends during high-luminosity illumination. Such illumination rhythmically and predictably modulates the ambient illuminance and color temperature, making it easy to sense on the printed PCB abruptly rising pulsed signals. The rejection of ambient light excursions lower than the values would allow instant demodulation of intended modulated received pulses, simultaneously from all the transmitted light source components.

6.3.2. Energy Harvesting Techniques

The most sustainable systems, if not all, are the ones that harvest energy from the environment to increase their lifespan indefinitely. The growing trend towards autonomous systems for the large-scale monitoring of the environment and the Internet of Things applications demand battery-free operation modes, thus imposing the need for adopting Energy Harvesting techniques. Energy Harvesting is the process of extracting the naturally available energy that is usually lost in the environment and storing it temporarily into various storage units for further use. The Energy Harvesting sources available nowadays range from ambient Light, Radio Frequency signals, kinetic energy, vibration, high temperature difference, ultra-violet radiation, mechanical energy, and electrostatic effects, magnetic effects, Peltier effects, acoustic energy, chemical energy, and atmospheric energy.

Solar Photovoltaics is still the most popular Energy Harvesting technique, with a growth rate higher than 20% annually, but are often a prohibitive solution due to their bulkiness and cost associated with the material and the complex fabrication technology. Thermo-electrics are also a valid solution but at the cost of device complexity and fabrication challenges. Piezo-electric Energy Harvesters offer low power levels but at a low fabrication cost and high degree of flexibility, thus becoming unsuitable for applications requiring a high degree of design freedom since large footprint devices do not reach the high output power levels typical of other Energy Harvesting techniques. On the other edge of the Energy Harvesting camp are the Electrostatic Energy Harvesters, that offer high Density of Power over the whole used frequency of vibration, but that lacks of

robustness when put directly in contact with the vibrating Mass since most of the Energy is lost in the dielectric injection, thus becoming suitable only for hybrid systems.

6.4. Sustainable Power Management Systems

An equally important functional aspect of the circuit architecture is the performance and economic overhead of the power management systems. Power management employs active and passive components on chip to help maintain a low power dissipation. In an ideal case, the PMU engaged in exhaustive power dissipation would be implemented, however, this leads to not only high hardware costs, but would also become a limiting factor in regard to performance and reliability. Static Voltage Dropping can assist in maintaining a low power dissipation and is one of the basis steps that can be taken towards energy efficiency. Advanced classes of PMU like Dynamic Voltage Scaling provide advantages over static droop methods by allowing the chip to change its voltage domain depending on workload requirements. A step further into customization of the PMU can be found in the Dynamic Frequency Scaling problem.

Dynamic Voltage Scaling

Power dissipation drops as either voltage or frequency is reduced, on a non-linear relation. Therefore any voltage reduction allows frequency drops allowing a temporary low power situation. It serves as a valid energy-saving concept for chip workload subjected to temporary spikes. Static Droops can be found in battery operated devices like mobile phones during standby periods. Over the last years, DVS techniques have been investigated using slow VTC and synthesis techniques. DVS Hardware approaches have found their way into several application processors. Many multimedia processors provide intrinsic DVS capabilities. Applications for these devices implemented with DVS optimize the battery time, because user-scheduled deadlines are present in the input data.

Dynamic Frequency Scaling

Reducing the inherently diselectrical device switching capacitance while maintaining chip logic capabilities has turned into a difficult task for silicon technology. Volatile memory cells and spin wave based technologies would lead to smaller capacitance compared to static CMOS. CMOS at the same time has the widest technological access and is therefore expected to stay leading with regard to non-volatile static components.

6.4.1. Dynamic Voltage Scaling

Energy versus performance remains the key challenge in designing modern circuits, especially at lower nanoscale technologies. Moreover, with the ever-increasing consciousness toward "green" computing where carbon footprint of the circuits should also be considered, this challenge has become even more difficult to tackle, as current solutions become more inefficient at lower technologies. Apart from using various energy efficient circuit architectures, many operating/supply voltage based methods such as dynamic voltage scaling, dynamic frequency scaling, power gating, etc., have been explored to mitigate the energy challenge. These techniques utilize run-time variations in speed and power consumption, and thus energy during execution of programs to combat the energy drain of the circuits.

Dynamic voltage scaling is the most widely used online technique where the operating voltage is varied at run time. DVS takes into account several voltage-frequency pairs, and decide at run time the appropriate voltage for the critical section of the program, so that overall energy during execution of the application is minimized. However DVS requires special voltage droop tolerant circuits as well as non-ideal voltage converters and thus leads to extra overhead as well as circuit design complexity. The other limitations of DVS is that it is not very power efficient at the lower Nmos-Pmos size ratios as is the case during low voltage operation, and cannot be applied to circuits and testers which are input vector insensitive and are thus directly related to the physical integrity of the circuit and the tester. Further for switched capacitance dominated circuits, lowering the supply voltage reduces the switching energy quadratically. However for non-switched capacitance dominated circuits, for example at low frequencies and even DC operation, DVS is not power efficient as the short-circuit power consumption becomes dominant during switching.

6.4.2. Dynamic Frequency Scaling

Active power consumption in digital CMOS circuits can be reduced by lowering the supply voltage. The average switching power of a CMOS gate is proportional to CV^2f, where C is the output capacitor, V is the power-supply voltage, and f is the frequency of operation. Static power dissipation, which is a dominant component of total power dissipation in technology nodes below 90 nm, is only linear with supply voltage; hence, voltage reduction yields a greater percentage reduction in active power. Low-voltage designs enable significant power savings, especially at low frequencies. As CMOS technologies scale and the frequency of operation increases, the dynamic power component becomes the main obstacle to further voltage reductions. Unfortunately, the lowering of Vt, which is required to boost speed and enable higher-frequency designs, results in a larger leakage component, which limits the voltage that can be applied to the

circuit. The method of dynamic voltage scaling (DVS) circumvents this limitation by allowing the power supply voltage to be varied throughout the computation.

Unfortunately, the global power management system that implements DVS must use voltage-level shifters to match voltage levels of circuits that are not operating on the same frequency domain. These overhead circuits introduce a non-negligible delay and power penalty into the design and also limit its scalability. Similar to DVS, dynamic frequency scaling (DFS), also known as frequency-voltage scaling, provides additional power savings by allowing the circuit's operation frequency to be varied at run time. Design techniques for strategies to allow frequency pitching at both the macro- and block-levels in multiprocessor systems, to allow parallel and serial partitioning of the workload, to support parallel I/O operations at reduced frequency, contention-free data access and memory modules with built-in support for dynamic frequency scaling in code-and memory architectures are examined. This architecture-dominated process attempts to provide its associated compiler and operating system layers with the design tools that are required to support the required software strategy so that a custom solution is provided for a target set of applications.

6.4.3. Power Gating Techniques

Power gating techniques are increasingly being used or considered in conjunction with other power-saving techniques. If well managed, this will help decrease leakage power without increasing dynamic power much. If appropriate techniques are used, they can even lower dynamic power. These techniques have been developed for specific power-management software and hardware. Initially limited to long break periods, they can now even manage shorter power-off times. Dedicated chip capabilities have been developed to improve energy management.

Standby power gating requires points in the design where power can be removed. For example, there are circuits where power can be removed without affecting flip-flops and the resulting transistor network. The consequences are that transistor networks are not powered when there is no signal transition. Hence when there is a signal transition, the path will have the delays associated with not being powered. There are solutions for those longer paths. The possible energy savings depend on the logic being strained, the actual standby power values sensed, the ratio between the transition time and the structural-high path time, and the time in standby. The equations to estimate energy savings with low-power CMOS, 5V CMOS, and GaAs circuits are given. The computational simulation is complicated by the fact that both delay and energy dissipation are affected by the gate that is not powered. The presented results were obtained using experimental results from 5V CMOS and GaAs MNOS sample circuits.

For the GaAs circuits, the energy consumed by latched and unlatched circuits are provided, using a low voltage. The total error rate for both devices is given when at latch.

6.5. Low-Power Design Techniques

This chapter has discussed various circuit techniques that help minimize energy consumption. This section discusses some additional design techniques that focus on parallelism, temporal characteristics of the target application, data activity, data communication, and operating voltage. The primary parameters that influence energy dissipation are transition activity, signal swing, power supply voltage, and load capacitance. The higher these values are, the greater the amount of energy consumed. Given the structure of modern chips, process supply voltage, load capacitance reduction becomes difficult. Thus for a specific data path, the designer may have control only over the signal activity.

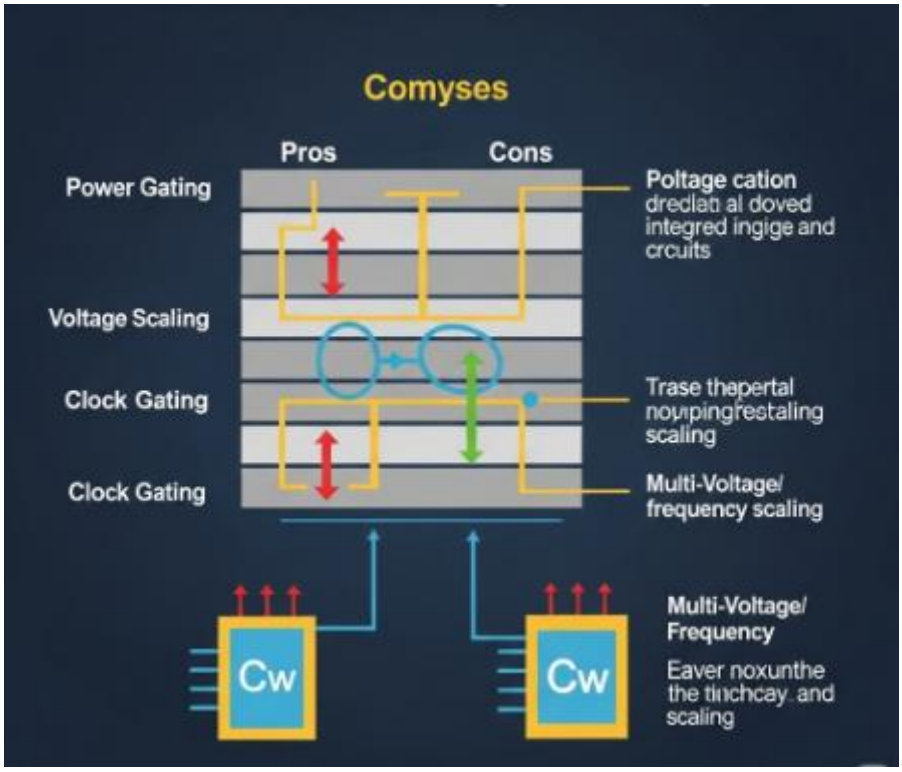

Fig 6.2 : Low-Power Design Techniques.

The static energy dissipation, on the other hand, is proportional to the supply voltage. Reducing supply voltage is one of the most common techniques to minimize energy dissipation, especially as technology scales down. However the limitations like noise

margins and process variations preclude the use of very low supply voltage. Additionally logic performance, including the performance of the leakage current, is also affected under very low supply voltage. The parallelism present in most applications allows for many alternatives in data processing. The possibility of processing data using different circuits at different points in time provides further for optimization of energy. These diverse effects exploit the controllable design parameters by decreasing signal transition activity, such as clock gating, data encoding, data packing concepts, and other design level optimizations such as sub-threshold operation. These methods can only affect the dynamic signal behavior of the design. However during the later phases of circuit design, high-level synthesis and architectural techniques can be employed to reduce the total load that is switched during processing.

Clock gating is a standard methodology at the RTL level and is also built into design tools. Clocks require the most amount of power in CMOS logic and adding new clock gating circuitry usually results in an increase in the total transitions in the design. Thus power aware design and proper investigations of synthesis reports will give the best results. Gate Level Clock Gating is allowed in most synthesis tools, but care should be taken when implementing it at that level in order to avoid glitches.

6.5.1. Clock Gating

Digital circuits spend a significant portion of their operational time in a quiescent state where certain functional blocks are inactive and produce no output for long periods. In order to reduce dynamic power dissipation, these inactive modes should also be disabled when not required. Historically, VDD was deactivated during these states; however, the problem with this approach is that the dynamic source and gate-drain capacitance associated with the switching of the PMOS or NMOS devices becomes a large fraction of the overall power dissipation during the transitions, thus diminishing the advantages offered by cutting off the VDD. Further, the VDD inverse rail to rail transitions cause large latch-up transients, requiring large devices to mitigate the problem; making it impractical for nanometer technology. To overcome this problem, clock gating was introduced, which uses the clock logic as the control enabling the local switches to switch the respective output signals. This has the advantage that at any given instance, only one output signal is toggling thus minimizing the overall dynamic power dissipation.

Clock gating is probably the most widely used technique in practice today, primarily because it can be independently applied to every functional block in the design, thus offering immense local flexibility. The timing of the enable signals can be made very selective by using special glue logic. Examples of timing circuits include state-machine outputs which enable the execution of operations only in certain states, instruction decode fields used active for a limited number of clock cycles during branch or load

execution instructions, or data path feedback paths which only allow data propagation from output to input for specific data, thereby enabling data synchronization to and from external memory. Clock gating is largely applied to the memory hierarchy, particularly because of the large memory access latencies employed in modern microprocessors. Nearly all caches today are clock-gated, asynchronous to processor access, yet on-the-fly on managed using dirty bit storage controllers.

6.5.2. Data Encoding Techniques

Data power management via circuit-level techniques can be implemented by limiting the switching activity at the inputs of a circuit. A common way to reduce the data switching activity is to encode the data-stream using a code that minimizes the switching transitions of the circuit. This can be achieved at an ancillary cost, in terms of area and/or delay, of the circuit which has to decode the incoming data and encode it before feeding the subsequent stage. The energy savings that an encoded data-stream can deliver permits to offset this area and delay overhead. Another assurance to the use of data encoding to minimize the switching activity is that the encoding/decoding circuits operate at a much lower frequency than the main arithmetic circuit. Therefore, the energy consumption associated with the activity of the encoding/decoding circuit is barely substantial compared to the savings in energy that the main circuit benefits from.

Several approaches have been proposed to exploit data encoding techniques to limit the number of transitions propagating through the circuit and reduce energy consumption. In general, as higher the resolution of the circuit, the higher the number of transitions that propagate through the circuit and the potential benefits from the encoding techniques. Data encoding methods operate primarily at three levels of abstraction. The first level comprises those encoding methods that modify the binary matrix associated with the function of the circuit to be implemented. The second level involves changing the circuit realization but without modifying the binary matrix. At a third level, data encoding techniques are applied after design or to a preexisting circuit.

6.5.3. Sub-threshold Operation

Reducing circuit supply voltage has many important advantages. However, reducing supply voltage does not reduce circuit dynamic power when the capacitance and frequency remain unchanged. The advantages of low supply voltage are mainly due to two effects: reducing static power, which allows other circuit characteristics to improve; and reducing dynamic power due to a reduced propagation delay time as supply voltage approaches threshold voltage. This basic idea of low-power design has obvious limitations. For circuit designs where circuit drive capability is critical, especially for

large fan-out circuits in digital VLSI, ultralow power is not a design priority. We can only cautiously reduce supply voltage to minimize leakage current, using the primary advantage of low supply voltage.

With the exponential dependence of energy on supply voltage, this approach may make little effect on dynamic energy dissipation as the supply voltage is reduced to very low levels. Dynamic energy is proportional to operating frequency or temperature. To achieve negligible dynamic power and energy dissipation, it is necessary to find methods to stop the logic or functional circuit from switching or operating. This has been conducted during the standby mode by using high-impedance input/off-state input gates that do not have load capacitances. However, low level noise can change the state of these gates and cause large static current in VLSI. The best way is to use voltage levels and currents much less than the noise margin, which will stop all circuit switching/operating activity during the standby and other modes. The static characteristics of MOSFETs and CMOS circuits allow designing circuits that operate in sub-threshold regions, where the FET conduction current becomes an exponential function of the applied gate-source voltage and small-signal transconductance.

A short way to achieve the above circuit behavior is to operate the logic gates and circuits at reduced temperatures, such as cryogenic circuits or low voltage organic circuits. If all gate and circuit dynamic transition states that apply gate-source signal levels were reduced to be much lower than the noise margin threshold levels, then the above requirements for negligible circuit dynamic power and energy dissipation may be drastically reduced by operating logic functions and circuits in the sub-threshold region.

6.6. Impact of Technology Scaling

Impact of Technology Scaling Integrated circuit (IC) design methodologies, tools, and architectures have always been developed in conjunction with innovations in semiconductor technology. The industry-wide push to scale VLSI technology, where the gates of integrated circuits get smaller along with the dimensions of the metal, gate oxide, and junctions, has driven exponential increases in the number of computational elements in an area during the past several decades and generated large benefits in performance and optimization for very large scale integration (VLSI) designers. Technology scaling, however, has not only posed many challenges in area, performance, and functionality. It has also created new opportunities for reducing energy consumption in digital circuits. Lower supply voltage and lower operating current per unit transistor associated with extreme nanometer technology scale down the energy per switching event in IC circuits. This fact along with the implementation gain of a larger fractal surface area of IC circuits containing nanoscaled transistors and active and passive

circuit elements placed on microscopic “real estate” in circuit building enables circuit and system designers to optimize the energy of operation per circuit urbanization.

6.6.1. Challenges in Scaling Scaling toward small dimensions brings potential pitfalls in extensive IR drop, increase in leakage currents due to tunneling, impact ionization and minority carrier injection processes, excessive gate delay, dominantly arising from below-threshold swing surges, severe process corner variations with dynamic threshold clocking, shorter time constant rc with degraded oxide capacitance and lower gate capacitance per unit gate area, reliability concerns due to hot carrier injection during repeated extreme reverse biasing, and random variations at extreme necking of channel junctions. Emphasis on developing new parasitic device models with more sophisticated predictive capabilities. More advanced thermal simulation modules for fast circuit level thermal simulations. Novel densification flows that can be applied efficiently in conjunction with the standard custom layout tools in chip physical and layout design phases. Chip power and clock pad design for testability. These are all compelling tasks that warrant joint effort by technology vendors, vendors, and users of tools.

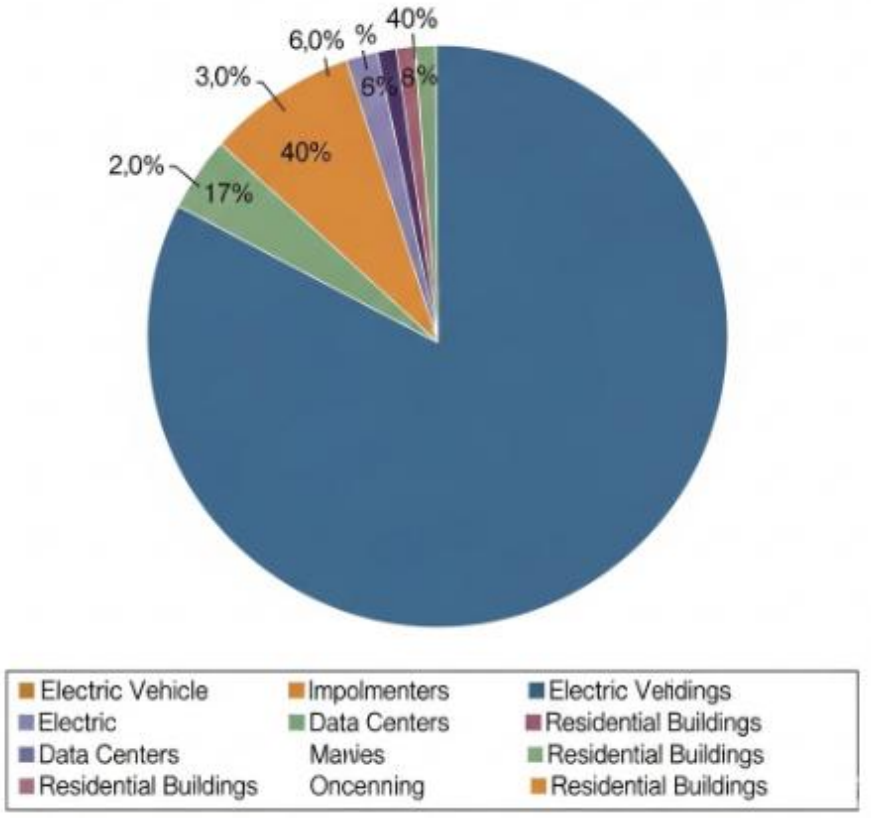

Fig : Energy-Efficient Circuit Architectures and Sustainable Power Management Systems.

6.6.1. Challenges in Scaling

The scaling of CMOS technologies has so far enabled increased integration and performance while offering reduced energy- and cost-per function. In the digital space, performance has increased with enhanced operating frequency and improved energy efficiency through dynamic voltage scaling. The DVS capability available in scales is advantageous to embedded applications like wireless, video, and imaging. These applications require high performance for limited periods of time and low power during idle periods, making it important to integrate these functions into a single system and not merely a chip. These trends of increasing integration density and decreasing energy per operation may not continue indefinitely in deep sub-micron technologies. Technology scaling is presently confronted with a number of fundamental challenges—sub-threshold leakage, increased variability, and corroding electrostatic control—that threaten to undermine transistor energy efficiency and operating voltage scaling.

Because of virtually non-scaling off-state currents due to leakage, low-threshold voltages can no longer be used in advanced sub-90nm nodes to achieve the necessary power and energy savings. The consequence is inappropriate off-state behavior that results in double the power required to run a circuit. Off-state leakage is expected to double every generation and become a substantial fraction of total active energy in ultra-low voltage circuits, significantly degrading circuit energy efficiency. Similarly, as short-channel effects become more significant in advanced scales, conventional approaches to using low operating voltage margins while maintaining high noise margins during active state are seriously challenged. Further, the high magnitude of design margin requirements required to overcome the effects of random variations in the transistor's characteristics are resulting in very large overheads on delay and energy during both active and non-active states, making the close to ideal direction towards reduced timing closure demand energy increasingly untenable.

6.6.2. Opportunities for Energy Efficiency

In the last few years, in addition to MOSFET scaling, there has also been a significant drive toward new device technologies, intended to provide enhanced performance, power efficiency, and density beyond that enabled by classical MOSFET scaling – so-called post-scaled design technologies. These alternative device technologies enable devices built on new physical principles or with different geometries, and appear to hold great promise for energy-efficient circuit architecture as well as power management. Usually, the motivation for this new device development is the breakdown of the principle of classical magnetism scaling relationships and the desire to overcome Burstein-Moss shift, enhanced degree of scattering, and SIE effects, which sets in when geometries are shrunk to deep nanometer dimensions. There are two new technologies

that are emerging fast and may enable energy-efficient circuits through the development of new device technologies that utilize the benefits of post-scaled device designs. These energy-efficient device technologies are graphene-only, or hybrid graphene/silicon enhancement mode CMFETs, with their very low ON-resistances and very high, energy-efficient performance figures, and also new device technologies based on alternative, lower-bandgap semiconductor materials that offer a good option to continue the advantageous scaling of CMOS through reduced gate capacitances, which in turn leads to reduced overall capacitance, and also preferably the price-performance of circuits based on CMOS technology.

These post-scaled alternatives not only allow retention of the advantageous device and performance scaling that was the driver behind several decades of scaling of classical device design, but even more importantly may also allow for a new era of elevated performance past the final scaling limit through a continued reduction in device gate capacitance. Therefore, this new class of energy-efficient CMOS technologies based on both alternative materials and advanced devices offers the very exciting prospect of addressing the energy efficiency of at-chip power management systems that will no doubt become increasingly vital for the economy, environment, and security of society in the near future as our societies become saturated with an increasing array of battery-powered portable electronics.

6.7. Conclusion

This chapter has highlighted the ongoing need for low power, energy-efficient circuits. The chapter began with a discussion of the Earth's increasing demand for energy, its own limited resources, and the impact of such energy use. This was followed by a discussion of some of the growing trends in hardware systems and applications, and the impact they have on future power requirements. Next, the chapter discussed the impact of voltage scaling on CMOS technology, and how it directly affects circuit energy requirements; however, reduced supply voltage and, in particular, decreased voltage swings limit circuit speed, and this has to be addressed. The discussion continued with the development of a number of methods focusing on reducing power consumption through various levels of voltage adjustment, for example, through the use of multiple voltage levels, dynamic voltage and frequency scaling, and adaptive voltage scaling techniques. The chapter concluded with a discussion of a range of future circuit design trends, including the development of new circuit families designed for low voltage and low power operation, a movement toward greater device parallelization, and the requirement for on-device energy-efficient power management systems, as well as multithreading and special hardware. This growing trend toward hardware developments is, in turn, focused on providing future devices with an increasing ability to deliver

connectivity, intelligence, and interactivity at any time and place; all while consuming very little power. Future trends within sustainable power sources were also examined. The technologies highlighted will be fundamental in realizing these goals, and the level of success we can expect of energy-efficient electronic and computer systems in the coming years.

6.7.1. Future Trends

Despite many enduring challenges connected to the continuing transistor miniaturization, in particular the inability to significantly reduce the runtime power drop and the ever increasing monoculture vulnerability of VLSI designs, which make overloads due to PVT parameter drifts and soft errors, among other things, a huge challenge for circuit designers, exciting technological and ecosystem transformations are happening in these times. The combination of silicon photonics, memristor based new devices and systems, beyond von Neumann architectures that efficiently integrate processing and storage, quantum and hybrid quantum-intrinsic classical computing, neuromorphic unconventional computing based on brain inspired architectures and rich heterogeneous ecosystem able to close the perception action loop, secure computing exploited by all optoelectronic destruction proof systems, autonomous and self-healing systems and layers, maturation of vertical integration technologies, radiative cooling as opposed to air-cooling of chips, fast quantum-network interconnected systems, major breakthroughs on chip and system level energy harvesting, nanowire and lamellar structured composite thermoelectric energy harvesting, pristine materials based cooling, ultra-low-cost and reliable monitoring of PVT conditions including soft error, RF, 100, 300, 1000+ and low Test and Validation overhead monitoring, integration of hardware and software low overhead and self-tuning techniques to run workloads on always the lowest, same or not operating voltage, and in general, movable and low overhead self-healing and self-sustaining detection circuits, are potentially game changing developments. These jointly with new architectural and societal paradigm shifts, particularly those in the shared economy and the experience economy, can strongly limit the explosion of systems complexity and systems scale while ameliorating the overall security.

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