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Chapter 1: Understanding the core physics and fabrication techniques behind modern semiconductor devices

1.1. Introduction to Semiconductors

Wide bandgap semiconductors (e.g. GaN) and semiconductor heterostructures (e.g. AlxGa1−xN/GaN) are the key wide bandgap semiconductor technologies in the twenty-first century. The one-dimensional photonic structures (OPSs) play increasingly important roles in the design and fabrication of light-emitting diodes (LEDs), lasers, and semiconductor detectors. Conventional LEDs and semiconductor lasers based on planar designs, however, suffer light extraction inefficiency in LEDs and spatial hole burning (SHB) and "hard" thermal fold catastrophes in lasers. These limitations can be overcome effectively with the use of OPSs which are formed by building the semiconductor heterostructures or directly integration with the photonic crystal design. This chapter presents the state-of-the-art designs and fabrication techniques of OPSs based on oriented growth of group III-nitride semiconductors for LED and laser applications (Amuru et al., 2022; Jouppi et al., 2023; Ning et al., 2024).

In the mid-twentieth century and the mid-1990s, the development of the technology and/or materials for a light source transitioned from gas discharge to early semiconductor devices (p–n junction LEDs), to the first generation of semiconductor lasers (e.g. InGaAlP lasers), and to visible and ultraviolet (UV) LEDs and lasers based on the wide bandgap semiconductors (e.g. GaN). As a result, remarkable improvements on economically important applications such as full-color flat panel displays and Blu-ray players. The state-of-the-art group III-nitride semiconductor technologies grown on the low-defect-density c-plane sapphire substrates and their vertical configurations (e.g. flip-chip structures) have enabled revolutionizations of numerous solid-state lighting (SSL) applications and civilian and military optoelectronic devices. Zero-thickness adjustable photonic crystal (PC).

The optical and electronic properties of two-dimensional (2D) materials are reviewed focusing on Monolayer and few-layer transition metal dichalcogenides. The conceptual understanding of how the dimensionality of the material affects its light absorption and emission, charge transport, and energy relaxation mechanisms is summarized. The strongly localized charge carriers excited by high-energy photoexcitation influence the optical response of 2D materials in important ways, a feature that could be explored for applications in optoelectronics. 2D semiconductors represent an important step toward the realization of miniaturized and portable electronics, optoelectronics, and photonics. 2D layered materials are attractive alternatives to bulk counterpart semiconductors for nano-sized devices due to the high on/off current ratio, ultrahigh carrier mobility, as well as gating effect (Shastri et al., 2020; Samuel, 2024).

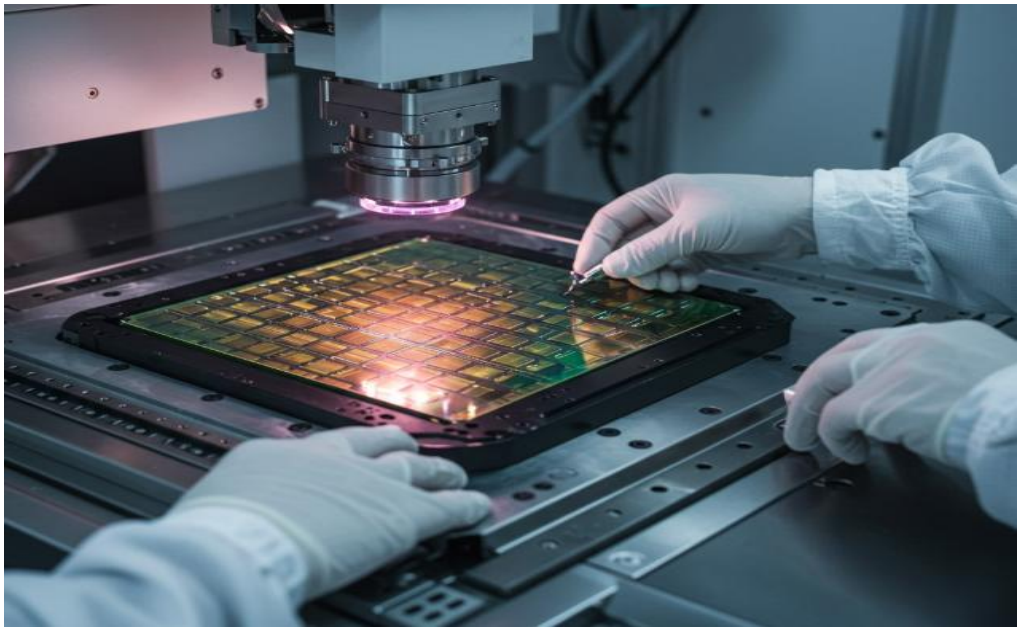

Fig 1.2: Semiconductor Device Fabrication

1.1.1. Background and Significance

Microelectronics technology has become a strategic technology globally attributed to its ubiquity in many aspects of life. Such ubiquity is reflected in, for example, the rapid convergence of information and communication technology, and the global production network. Microelectronics is thus a key pillar industry for many countries. Yet, the democratizing technology of microelectronics was, and is, both an outcome of and a necessity for the emergence of the information age. Growth rates of microelectronics are

orders of magnitude larger than those of GDP across regions and countries. Such growth has profound implications for scientific productivity and for finance and public policy.

The microelectronics revolution has been enabled and driven by the steady scalability of the silicon transistor as well as the computational efficiency of its complementary metal-oxide-semiconductor architecture. In pursuit of cheaper, faster, smaller, and more power-efficient electronics, the transistor has evolved from an onion-shaped planar device with minimum feature size of 10 μm in 1971 to a three-dimensional device with gate-all-around architecture and attained minimum feature sizes of 22 nm as of 2013. Improvements in Mr. Moore's Law predictions suggest that continued scaling is feasible at least for another decade. Greener architectures based on manycore chips and non-volatile memory are also being explored.

Despite such successes, many interrelated scientific and practical limitations render this ever-narrowing pursuit of scaling increasingly difficult.

1.2. Fundamental Physics of Semiconductors

The first-principle understanding of semiconductor devices developed in this handbook is rooted in recent advances in theoretical as well as computational techniques in many fields of physics, starting from the early days of quantum mechanics and quantum field theory. This provided the framework and apropos tools for investigating a wide range of nanostructured systems, many of which have been realized experimentally, and some of which are of striking technological interest. In the physics literature, comprehensive subjects of nanostructured systems have been extensively treated, many advanced characteristics and phenomena being uncovered, including their quantum phenomena, quantized conductance, level spacing, neutrality point scattering, quantum interference, thermoelectric response, laser properties at nanoscale, to name just a few.

Semiconductor devices in the form of nanostructured materials, heterostructures, and nanostructures have inspired widespread interests in both the scientific and technological communities. In this regard, supplemented by the relevant novel fabrication techniques, remarkable step forward has been achieved particularly with respect to the understanding of their electronic and optical properties. These aspects include, amongst others, the conventional quantum mechanics-based understanding of the energy band structure, or conformations of the electronic energy states resulting from the interatomic interactions, confinement potentials, and their inhomogeneity and disorder, or localization and scattering processes of the carriers.

1.2.1. Band Theory

Over the last couple of decades, improved understanding of the microscopic physics of solids has paralleled the development of increasingly sophisticated methodologies for studying solids and their properties. The improved understanding has arisen from bridging the gap between the mathematical formalism of quantum mechanics and the crystalline structure that is ubiquitous in nature. Knowledge of the structure can be correlated with the way structures perform. In an applied sense, a solid can be thought of as a three-dimensional periodic arrangement of atoms. The atomic positions define a set of lattice vectors that leads to a lattice, a simple, periodic geometric structure. The arrangement of atoms within a unit cell defines a basis that, together with the lattice, leads to a crystal. Crystals are described with pseudopotential-band pictures based on density functional methodology. From the band structure, a picture of semiconductor physics appears with wave-packet parameters describing the state and motion of a particle. For clean semiconductor band structures, the eigenfunctions can be viewed in the tight-binding approximation as superpositions of localized atomic orbitals. The eigenfunctions form a complete set of orthogonal basis states for the Hilbert space on which the Hamiltonian acts.

1.2.2. Charge Carriers

In solid-state devices, the charge carriers are removed from their atoms or molecules and move freely through the material. The solid can then conduct electricity, and depending on the charge carriers, it is referred to as a conductor if the charge carriers are electrons and an ion-conductor for positively charged holes. The elegant ambipolar transport of opposite charge carriers gives rise to a dynamic recombination and thus, a longer charge carrier lifetime compared to unipolar devices. These processes happen on a large variety of spatial and time scales and can be divided into three distinct regimes.

First, the drift and diffusion of the charge carriers in the bulk, which are about a few centimeters (cm) in distance and typically less than a microsecond (μs) in time. The drift of the complimentary charge carrier species to the other electrode can be measured via an external circuit. The resulting transit time gives access to the charge carrier mobility. The charge carrier dynamics in the bulk can be probed via a small-signal approximation based on the linearized Poisson's equation and the continuity equations. Note that for a steady state drift-diffusion model, the effect of the electric field on the charge carrier dynamics is neglected, but since the drift-diffusion equations are non-linear, steady state holds in a quite large range of voltages, charge carrier densities, and material parameters.

Second, the charge transport in the semiconductor-electrode interface region (the Schottky barriers). Transport depends on the semiconductor's thickness, and by varying

the thickness in a set of otherwise identical SCLC diodes, the charge carrier mobility in the semiconductor can be determined. A special case of the competition between bulk and interface limited transport is the so-called injector dominated charge carrier transport that occurs in single-carrier-devices where both contacts are of the same work function. Before a bias voltage is applied, the system is at equilibrium and no current flows. Contacting two materials of different work functions generally leads to a flow of charge carriers between the two materials until a flat chemical potential has been achieved. In the case of n-channel operation of a material with an electron affinity less than 4.2 eV, the semiconductor possesses a higher work function than the metal. Holes traveling from the metal into the semiconductor thus have to overcome a Schottky-barrier, impeding the charge transport. After a bias is applied, the system acts as a high-resistance capacitive divider.

1.3. Types of Semiconductor Materials

The most common semiconductor material bipolar junction transistors (BJTs) are AlGaAs, GaAs and Si. In this chip, there are two types of materials, one type has been doped by any element then they are called n-type or p-type materials, corresponding to electron or hole carriers. The other type is intrinsic material, which has not been doped and mainly based on Si. Because of these structures it could form an np or pn junction which is essential for device operation. The hetero structures are made from different semiconductor materials; each layer of different material has a different colored shadow. This means that one or more materials are composed of many layers stacked up to form a heterostructure (> 5 layers), the vertical stretch is 5 μm is not large compared to the lateral size (mm). Typically, these layers are first defined by photolithography forming the splitting capacitor, which is the mask to grow the semiconductor material. The formation of a mask also yields an isolation from the substrate by forming oxide capacitors or buffer layers. Nowadays, the most commonly used semiconductor materials for optoelectronic devices are direct bandgap III–V hetero structured materials. Direct bandgap materials have the upper conduction band and lower valence band parabolic shapes thus it could conserve the momentum of photon carriers, as a result, more photons are emitted due to the faster recombination of electrons and holes. Bulk direct bandgap only existed in thick III–V materials. Taking reflectivity epitaxy as an example, light emitted from a bulk semiconductor would lose 80% of the emission, which is inefficient for application. But instead, one or more monolayers of WLs could be epitaxially grown on the top of the bulk direct bandgap semiconductors. The thickness of which <1 nm in monolayer materials is on the order of the wavelength of ultraviolet light 253.7 nm is thus expected to significantly enhance the light extraction efficiency for optoelectronic devices.

Binary group IV semiconductors, such as silicon, germanium, and their alloys heterostructures, are the main materials used for a variety of semiconductor electronic devices, such as field-effect transistors, radio-frequency transistors, and light emitting diodes. These conventional devices rely on silicon and germanium elemental materials. Such devices, however, are inherently limited by their thermionic mechanism that makes them slow, bulky, and metallized and thus unsuitable for information processing. In contrast, group III-V semiconductors and their devices are becoming increasingly popular due to their superior speed and performance. However, their fabrication is complex, and the intrinsic materials are costly and environmentally unfriendly.

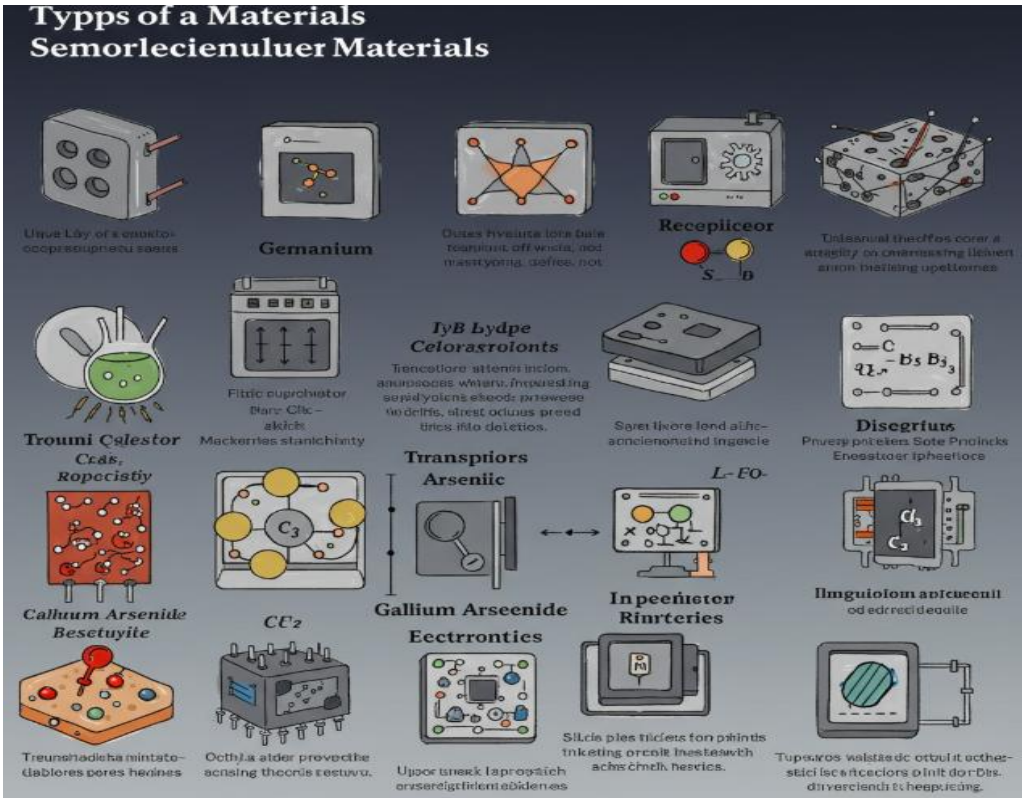

Fig 1.2: Types of Semiconductor Materials.

1.3.1. Elemental Semiconductors

The discovery of a metallic monolayer phase of silicon has attracted considerable interest because of its potential applications in nanoelectronics. Similar to graphene, silicene is predicted to support a large spin-orbit gap under an external electric field. Devices based on this material or its nanostructures could be used for seeking electrically tunable spin transport, logic operations, light modulation, or future analog computing. Like graphene,

the electronic states in silicene monolayers host a Dirac cone structure, supporting massless Dirac fermions.

Silicon atoms can also adopt a new planar structure that is stable under ambient conditions and possesses a linear dispersion relation. Fabrication methods have been proposed to obtain free-standing silicene, a new type of carbon-free material that can be readily integrated with Si nano-electronics. Silicene nanoribbons with periodic chairs exhibit no edge states and electron confinement can be engineered through pulsed gate voltage.

Recent work has shown that silicene and related two-dimensional structures are able to poly-crystallize and this is desired because ecological challenges arise during applications of monocrystalline materials and their hardness difficulties impede scalability. From energy-based structures, properties of monolayers are far less studied; while confinement can result in various stable conformations for polycrystalline monolayers, the energy landscape also provides many avenues to control electronic response dynamics and to stabilize novel structures and phases.

Most oblique angle deposition devices are deposited on smooth substrates, as the dielectric materials must be thin to allow direct contact for the first deposit. As the first level of the device is more or less planar, the ideal thickness and a fully insulated path on silicon deter the deposition of the dielectric materials. For integrating devices with different dimensions, avoiding needing mechanical and chemical polishing is necessary.

1.3.2. Compound Semiconductors

One of the key aspects of transistors that have led to the growth of the modern semiconductor industry is the material that the transistor is made of. Bare silicon used to be the only semiconductor material that was heavily explored, but due to the increasing demand of high frequency, high power, and high temperature devices, there was a need to develop more advanced materials like III-V semiconductors. These group III and group V elements have better electrostatic control due to their high saturation velocity. Heterostructure devices using these materials exhibit high power, high frequency, and low noise figures due to their sharp band discontinuities ensuring better electrostatic control. These devices are widely used for telecommunication systems and under extreme environments. However, most of these complex structures cannot be realized using bulk substrates. It has been a decade-long challenge to fabricate devices on silicon substrates where performance performances can be optimized and the cost can be reduced.

Inner side walls are used to realize an undercut channel, which is combined with a GaAs wet etching process for the fin sidewall in a surface-micromachined field-effect

transistor (SM-FET) structure. These have been fabricated on a silicon substrate instead of the gallium arsenide substrate. This approach enables the novel silicon-type micro-fabrication technique to be applied to compound semiconductor devices while keeping their large scale fabrication compatibility. A combination of a low thermal expansion alloy and a Mei-Osaki technique can ensure the reliability of device transfer owing to the reduction of a loss of adhesive strength. In transformation from gallium arsenide to silicon, new physical mechanisms are introduced to observe switches, making it feasible to prepare useful nanocrystalline silicon-based FETs. These results open up the possibilities for application of novel micro-fabrication techniques to compound semiconductor electronic devices for high-frequency applications.

1.4. Semiconductor Device Physics

For high-performance computing (HPC) systems, pervasive computing, consumer electronics, and sensor systems, semiconductor electronic components—transistors and diodes—are used in large numbers as critical devices. In processors, they enforce a digital logic and implement multiplex logic, adders, and memory storage, while transistors in diodes, mixer or oscillators, or amplifiers fulfill RF analog functions. More generally, transistor-based amplifiers are the heart of nearly all sensors, starting from MEMS accelerometers that exploit capacitive sensing to hybrid infrared sensors that combine ambient-light and temperature sensors along with pixel-based CMOS image sensors. Each of those devices corresponds to a well-defined physical principle that provides functions exploited in integrated circuits. Such local properties are essential to the understanding of device fabrication processes that must start from a lucid understanding of the local physics governing the chosen semiconductor device technology to materialize its desired large-signal behavior.

Most common semiconductor technologies consist of layers of Si and SiO2 either conventionally deposited or integrated through a far more complex approach with several materials used for the implementation of various functions. On top of the geography of the lattice, semiconductor research for more than the past fifty years has focused on new dopants, impurities or defects against which modeling efforts take a greater or smaller extent. All these topics give insight into the scaling laws adopted to fabricate impressive density digital systems, but are too general to exploit the potential offered by the optimal combination of local properties and large-signal modeling. Literature dealing with specific devices such as complementary metal oxide semiconductor transistors (CMOS), photodetectors or MEMS devices provides a clearer insight into the physics behind them, but remains difficult to assimilate with respect to the craftsmanship of the local device.

1.4.1. Diodes

As one of the most ubiquitous electronic components, diodes have been intensively studied over the past century, resulting in lowered device performance. In contrast to silicon-based technology, researchers focusing on organic and printed electronics pursue the exploration of a new, eco-environment paradigm. Enormous efforts have been devoted to the search for fabrication techniques for printed diodes compatible with roll-to-roll processing. As an important step towards disposable, low-cost, and high-performance diodes, nanostructured oxides processed via flow-based methods such as inkjet printing and spray-coating have been developed because of the unique compatibility of oxide nanostructures.

This review summarizes the progress of recent advances regarding the material processing, fabrication, and applications of printed diodes, with an emphasis placed on the aspects of solution-processing and material performance. The introduction of oxide nanostructures boosts performance improvement, rendering them competitive with synergistic approaches such as p-n junction integration and modification of device structures using ultrathin films. Improved performance by diverse types of printed diodes is also introduced. The relative advantages and challenges for each type of device are discussed. Considering the unmatched production scalability of printed diodes and their intrinsic suitability for flexible and wearable applications, significant improvement in performance and intensive research in development and applications of the printed diodes will continuously progress in the future.

The Schottky diode is one of the simplest diodes in its simplest form, which consists of one layer of a p-type or n-type semiconductor positioned between two metal electrode contacts, one of which permits charge injection in one bias direction while blocking in the other. A large portion of printed diodes are single layer unipolar devices based on a single semiconductor of either electron or hole conduction properties. In the multi-layer structures, both the hole- and electron-transporting materials can be coated on the same substrate to form p-i-n style devices. No need for high temperatures for post-treatment nor expensive high vacuum deposition apparatus makes the solution-processable route to fabricate the low-cost step in the printed electronics area.

1.4.2. Transistors

Transistors are ubiquitous components of modern electronic circuits and circuits composed entirely of transistors, called transistor circuits, are the most frequent building blocks. Transistors are three-terminal devices, and diverse device designs are known, including field-effect transistors (FETs), bipolar junction transistors, and their both respective variants. Current modulation, the operation mechanism of transistors, is

difficult to achieve without the three-terminal layout since a two-terminal device can only turn the current on or off. To an even greater degree than their simpler counterparts, resistors and diodes, transistors are intricate circuits composed of many circuit elements. A complementary metal-oxide-semiconductor (CMOS) inverter circuit consists of four circuit elements – two N-channel and P-channel transistors, two resistors, and two capacitors. When each of these resistors are replaced by the simplest two-terminal device, two charging and discharging paths are created, making the circuit hugely complicated.

However, it should be remembered that active devices other than transistors exist. As a part of basic education, a two-terminal device called a memory capacitor is introduced. If a charge is once added to a capacitive system wherein one terminal of a capacitor is connected to a node '1' or at power voltage (P), the circuit can keep the voltage at node '1' even when the capacitor is disconnected from the power supply voltage. This is because a barrier well is formed to hold the charge and prevent the discharge. In other words, charge modulation, the operational mechanism of a memory capacitor, is achievable without the third terminal connection. There exist many other two-terminal devices that can modulate physical quantities such as charge, current, or light without terminal three: resonators modulating frequency of oscillation; memristors and memcapacitors modulating resistance and capacitance, respectively; photonic devices and light-emitting devices modulating light. However, none of them have a capability equivalent to transistors for electronically generating functionalities, regardless of complexity.

1.5. Silicon Wafer Processing

Silicon wafers are the most widely used substrates for fabricating integrated circuits (ICs). Nearly all microelectronic devices consisting of transistors, diodes, capacitors, resistors, etc., are fabricated on silicon wafers. Such devices have generated a larger economic impact than any other human made items, including automobiles, airplanes, pharmaceuticals and CDs. There have been continuous demands for larger diameter silicon wafers with lower prices due to the relentless trend to build higher performance ICs with lower cost. The well established Czochralski (CZ) based manufacturing processes for producing silicon crystals, ingots, and wafers in the 1990s were still capable of meeting the demands for 200 mm wafers. Nevertheless, since 2000, the performance gain ratio of IC devices manufactured on 200 mm wafers has slowed down, making it difficult to meet the user's demands for higher quality silicon wafers at lower prices. On the other hand, large efforts have been made to devise technology for the points separation of 300 mm wafers from crystal boules.

Along with the continued demand for larger diameter silicon wafers, there have also been demands for reduction of mechanical and electrical defects in silicon wafers and improvement of surface quality and flatness of silicon wafers since in the past. Over the past 20 years, impressive progress has been made on the surface processes, such as the lithography, oxidation, diffusion, ion implantation, wet etching, and CVD, used to process silicon wafers. However, the fabrication processes for silicon wafers, i.e. the wafer processing methods significantly affect the material quality and surface quality of the wafers. It is for this reason that continued research efforts are made on studying conventional fabrication methods for silicon wafers, such as ingots slicing, grinding, polishing, etching, lapping, etc., and searching for other methods. Currently, a 300 mm wafer is sliced into 40 wafers and lapped and polished with a throughput of about 0.06m/min. In order to industry standardize 450 mm wafers, their throughput would drop to 0.04m/min due to the blade breakage and a similar throughput of about 0.034m/min would be required for other methods. Hence, efforts have been made to study new methods to replace or enhance the conventional processes, such as wire sawing, PCSS cutting & grinding, ELID grinding, CFIP polishing, and nano polishing.

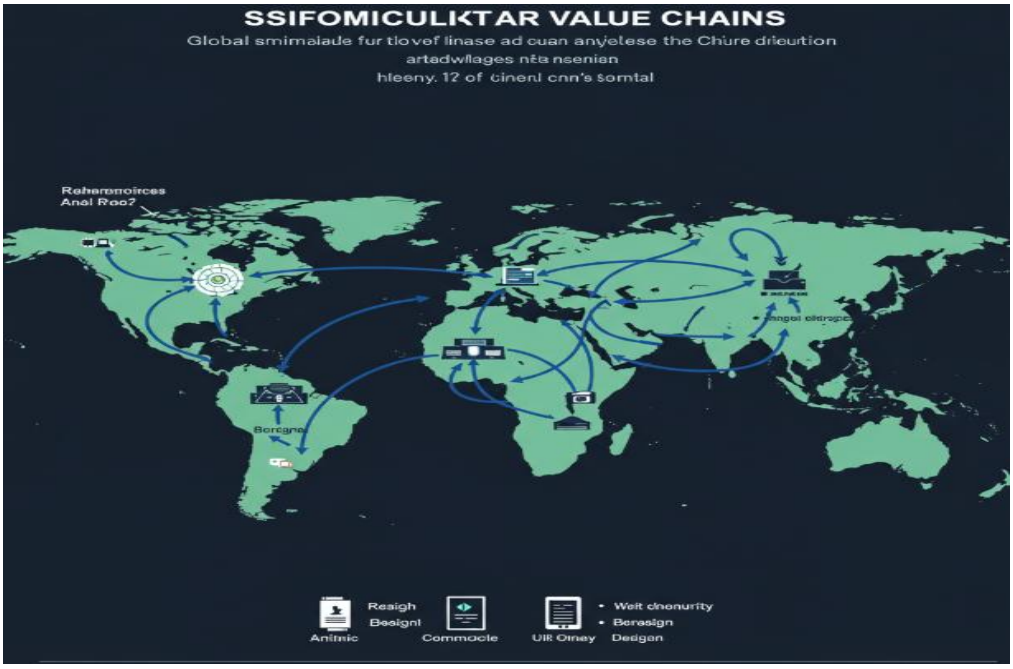

Fig : Global Semiconductor Value Chains

1.5.1. Crystal Growth

Crystals are grown from either a melt, a solution, or vapor, in a process best described as an intensive supply chain that involves carefully managing not only the growth and

shaping of the desired crystal, but also the careful purification of the starting materials and careful systems design necessary to avoid even minute perturbations in the growth recipe that would adversely impact the end-result. Crystals begin as “nuclei” (or nuclei), and systematic duplicates of them, referred to as “seeds” are developed. These seeds are accentuated perhaps 4, 6, or even 10 dimensions through growing the desired bulk crystal about them, precisely as various egg-like seeds grow trees, which despotically expunge any competitors in their vicinity. Leaves and hearty branches are developed by cutting the parent crystal into chunks, and metalizing those chunks into mini-anvils capable of copious pushing but an infinitude of pulling, the smarter leaves. The leaves are pressed against multiple sides of an active silicon substrate wafer, emulating a Fisher King story of a kingdom so large half of it adrift in the sea, requiring an ardent quest for a simple truth. Ribbons of metal-particles-embedded polyimide are pulled along tapering apertures of anisotropic aluminum and silicon, and shaped lengths deposited into shaped semiconductor stacks: detail beyond human understanding. At this point, photonics and magnetics enter in full force, supposedly to guide an electron photon to exhibit its raspberry bush like behavior within a lattice. While this is described loosely as “transportation”, transport cannot be computed in a practical sense, such as at room temperature for carbon nanotubes, given the exponential growth of the amount of “hidden” detail needed to develop such mechanical purposes in the timeline that activity develops. Instead, as with pictures of black holes, approximations with illustrative parameter bounds are developed to parametrize the illusions with messy spikes that forestall predictions which are embarrassingly short of words or diagrams. In all technical senses, these approximations are “theories”, though they renounce that term. Multiple paradigms animating “motion” concurrently and crisscrossing in a disgustingly entangled fashion are depicted as having machine-like beliefs, hats, swords, and fake children.

1.5.2. Wafer Cleaning

Wafer cleaning is the physical and chemical removal of contaminants on wafer surfaces of the semiconductors. These contaminants can be broad and can consist of organic, inorganic, and ionic contaminants. With the advancement in the photolithography technique, cleaning methods have to be suitable for high aspect ratio & sensitive surfaces, i.e. low-k dielectrics and porous SiO2. The current understanding and prevailing techniques of wafer cleaning need to be presented in this section.

The wafer cleaning procedure encompasses both the pre-drying steps and post-processing steps. The cleaning procedure is very dependent on the type of contamination and the job to be carried out. There is no adequate universal cleaning method available today. The procedures include chemical cleanings which are broadly electrocatalytic,

thermochemical, photochemical, plasma-assisted, ion beam, and supercritical fluid cleaning, and physical cleaning techniques. Wet cleaning has become the workhorse for wafer cleaning. Large batch tool cleaning has been replaced by aqueous-based single-wafer processes. Chemical cleaning techniques are specifically developed for silicon and have become part of the standard integration technology. Remnants from chemical cleaning are often not fully removed by conventional rinsing techniques. The most common types of contamination are inorganic, ionic, and isotopes that are based on ions.

The cleaning of inorganic and ionic contaminants relies on overall charge neutralization. Organic contaminants include hydrocarbons from natural sources, hydrocarbon-based photoresist from processing, and many other organic compounds. Organic contaminants are chemically converted to simpler, volatile molecules and/or oxidized to water-soluble fragments. In the standard integration procedure, the functionality of the wafer surfaces is changed sometimes several times. Hence the suitability of the surface conditioning technique widely employed for silicon must be demonstrated for these extended surfaces.

1.6. Conclusion

Semiconductor device dimensions have been decreasing steadily, from 10 μm in 1970 to 45 nm today, generating the need to overcome limitations of materials and fabrication techniques. Continuously growing requirements on performance provided by scaling according to Moore's Law led to the introduction of novel materials, work-functions and device architectures, but also increased the complexity of their fabrication. Modern metal gates consist of a stack of different materials, which can reach a total thickness of about 100 nm, requiring up to 15 processing steps for their formation. Of increasing importance for stable operation of such devices is access to accurate models that describe fabrication techniques and their limits, as well as the impact of defects and materials/material parameters on the predicted behavior. Computer aided design is an efficient and flexible solution for the description of physical techniques, which is well established in the circuit technology community.

Modeling the mechanics enables one to understand topology changes occurring as result of material removal, deposition and processing steps, for example, high angle annealing. This involves a trade off between complexity and efficient aspects of the mathematical description. Whereas the first part of this review discusses fundamental methods, the second part highlights common techniques for modeling transport of molecular entities, using either thermal or concentrated solutions, to accelerate the modeling of new relevant methods and materials. With modern chemical mobilities, common setups become computationally prohibitive and their limitations need to be carefully addressed. The modeling of surface chemistries involved in oxidation and chemistries for advanced

deposition techniques has enabled the identification of the dominant etch mechanism for multiple materials. Recent accomplishments modeling the kinetics of a polysilicon etch process are discussed, as well as advances in the description of a proprietary dry oxide deposition process.

Recent advances made in the modeling of gate stack pattering, using advanced geometries of masks and developing sophisticated chemical models are discussed. Such techniques require and hold various types of numerical options, a variety of methodologies and methodologies not yet publicly available, which cover a broad spectrum of represented physical processes. For their general practical use, the applied methods are briefly discussed, as well as the consideration and tuning of model parameters needed to achieve reliable predictions. Finally, existing options, needed added capabilities and integration of distinct methodologies are considered to overcome some limitations and improve understanding of technologically relevant processes, especially those involving transport and chemistry.

1.6.1. Future Trends

The National Academy of Engineering lists, "Make solar energy economical," and "Provide energy from fusion" as among the greatest challenges of engineering in the twenty-first century. Moore's Law is predicted to end around 2025 due to rising power dissipation. In the last forty years, conventional transistor technology has been forced to use increasingly complex and exotic methods to solve the grand challenge posed by Moore's Law. However, there are fundamental limits to this approach. Photons hold the greatest promise of taking semiconductor technology to the next plateau. Orders of magnitude increase in performance and smaller devices are possible with silicon optical devices. Fundamental questions must be addressed for scalability and realization of the silicon optical circuit.

The promise of silicon photonics is based on the expectation that silicon and its oxides will serve as a technological platform for large-scale integration of optical and electronic chips, operating at near-infrared wavelengths at or just above room temperature. Signals on such circuits will have place-and-route-optimized routes to interconnect densely packed high-speed CMOS transistors. Silicon photonic waveguides will replace copper interconnects. Ideally, the photonic devices need to be real estate efficient, power efficient, and compatible with the CMOS manufacturing infrastructure. Optical devices that fulfill these requirements will also show new functionality and integration capabilities not possible with electronic devices.

Static routing is highly scalable in silicon technology. In addition to real estate efficiency, interconnect density, speed, and power dissipation, capacity can be enhanced

with the use of broadband dynamically reconfigurable optic-electronic networks-on-chip. Eventually if real estate efficiency is satisfied, those chips can be much larger than current chips and again all of the off-chip bandwidth can be used electronically. There are fundamental challenges to be surmounted before these visions can be realized.

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