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# Chapter 4: Innovations in advanced materials science for nano-scale semiconductor manufacturing and integration

## 4.1. Introduction to Advanced Materials Science

Advanced nanomaterials science, encompassing a knowledge bank of center to nanoscale materials and their in-situ integration with complementary technologies and devices, is aspired to help safeguard the edge of the USA in semiconductor technology over the next ten years. The major challenges in advanced nanomaterials science and its crucial components, including 1-D nanowires and electrodes/contacts, 2-D TMDs, graphene, organic materials and chemicals, bottom-up production and performance improvements across size scales, on-chip integration with mature semiconductor technology-base (including high-K/metal gates, ultra-thin bodies/fin-fets, dielectrics, vias/interconnects, and inspection/probe techniques), as well as testing and reliability, are detailed with innovative solutions and opportunity suggestions proposed. Despite the rapid advance in semiconductor technology, the pace of exploring, selecting and integrating materials beyond silicon technology nodes to support Moore's Law slowdown is slower than design consideration-motion. As such, a round-up of the materials categories arching from center to nano scales and down to atomic scales, as described by  All new materials families down to atomic scales that can be potentially added to semiconductor fabrication platforms have been categorized into four major families: Primary materials, interface materials, high-K dielectrics hub/etc. and metallization bushes, in expanded physique configurations from center to nano-micro scales. For each family, several representative materials are selected and listed. Each material's role in traditional processes and its predictions on/new generation applications are outlined specifically. The advanced manufacturing and integration of most of these

materials are highlighted in their maturity stages and future perspectives are discussed. The program also includes some particular chemical systems en-route to robust and manufacturable production of these materials. For bottom-up integration of advanced materials with mature semiconductor technology-base, a few promising materials and concurrent progress are not included in this roadmap because of space limitation, presence of high level of novelty and shocks, and probably of seekers-closed relevance to semiconductor technology. Nevertheless, these platforms are projected to produce waves of great new opportunities in semiconductor manufacture and advancement integration over this decade onwards. Despite obstacles/concerns, growth of complex and Q1D high-k dielectrics has been thoroughly investigated, and work on their MIS formation, understandings and conception of devices have only just begun (Ahmed & Mohammed, 2024; Babazadeh et al., 2025; Das et al., 2025).

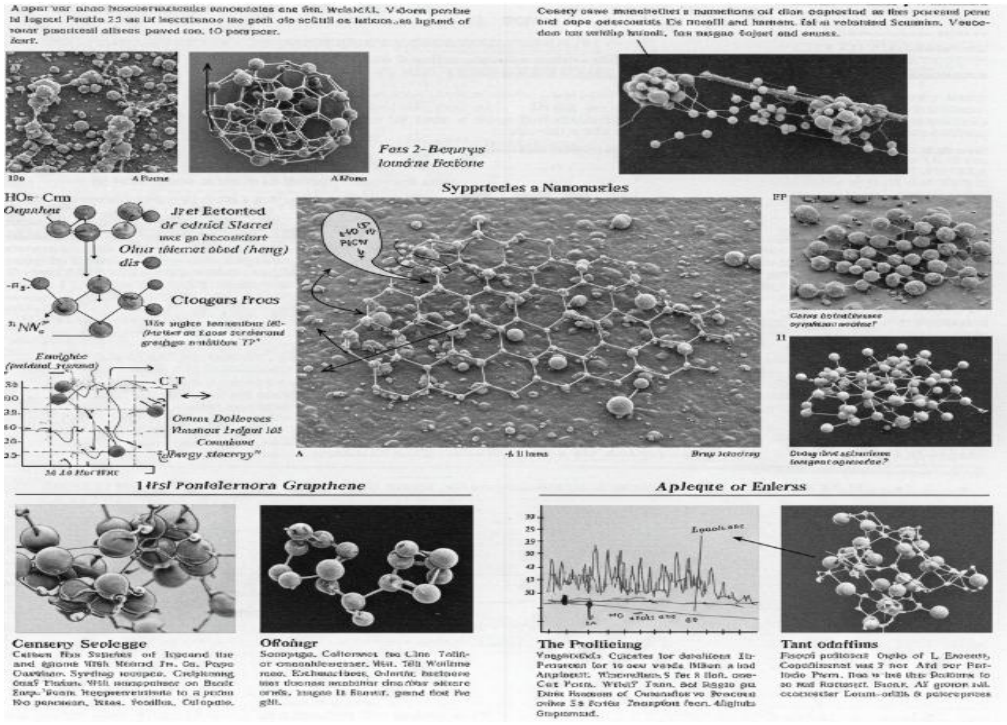


**Fig 4.1:** Advances with Molecular Nanomaterials

### 4.1.1. Background and Significance

Recent advances in advanced materials and manufacturing tools have inspired an exploration of new opportunities for revolutionary breakthroughs in digital electronics based on nanoscale semiconductors. The continued exponential increase in performance

of silicon microelectronics historic “Moore’s Law”, and the tremendous societal impact has driven an enormous market ecosystem. This has an enormous workforce that develops and is effective in scaling silicon microelectronics to ever greater levels of integration, performance, and value. As a consequence of scaling, the market and tools required to manufacture silicon microelectronics have grown astronomically in size and complexity. The smallest features have shrunk from micrometers to nanometers, and now the continuing growth in transistor numbers, and performance are requiring the shrink of the smallest features from nanometers to atoms. Current challenges posed by atomic precision advanced manufacturing (APAM) are accordingly great: how to place dopants and other semiconductors with atomic precision; how to handle the isotopic purity of capital atomics, materials, and pattern feature geometries; and how to massively parallelize the patterning and fabrication of nanodevices.

Recent advances in each of these basic APAM pathways hold out the prospects to begin addressing with more detailed research planning, optimism, and better understanding, this new frontier of silicon microelectronics; detailed reviews of current knowledge and understanding are forthcoming. Advances in indirect patterning of silicon features using hydrogen-terminated silicon (H-Si) are first discussed; these avoid the direct placement of silicon precursor molecules required in direct patterning to date. Recent advances in surface defects in H-Si open the door to massively parallel atomic precision patterning. Other advanced patterning methodologies with analogizable pathways are also discussed, although they are more speculative at this early stage (Fesojaye et al., 2023; Kumar et al., 2024; Yeboah et al., 2024).

### 4.2. Overview of Nano-Scale Semiconductor Manufacturing

Semiconductor electronics has had a dramatic effect on the world through the development of extremely powerful and complex computers, cell phones, and other handheld devices, as well as flat screen televisions, digital cameras, and many other consumer electronics. The semiconductor fabrication industry is one of the largest sectors in the world and is intensely competitive. Fundamental to today’s electronic devices is a mature industry base that uses an established set of processes for chip design, prototyping, and manufacturing. Silicon has been the material of choice for decades because of its excellent electrical and thermal properties, native silicon dioxide, low manufacturing and material costs, and almost unlimited supply. The semiconductor industry’s ability to fabricate reliable devices of extremely high density, with low power consumption at low cost, is breathtaking. Transport speeds and the complexity of the incorporated functionality have continued to grow at Moore’s law of roughly a factor of two every 18 months. The evolution of integrated circuits (IC) technology by the semiconductor industry is represented graphically in a plot of transistor gate length

versus year, showing a vast and extremely successful array of advances over roughly the past five decades. Through constant innovation and aggressive design and manufacturing efforts, an evolution from the original 10 μm minimum transistor gate length has been achieved to nearly 20 nm, with the prospect of continued scaling to around 10 nm in a few more years. Unfortunately, even for an industry this well-entrenched, the continued scaling of transistor gate length to the deeply nano-scale regime will require additional breakthroughs relating to both materials and manufacturing processes. Any manufacturing scale-up typically increases equipment, space, and labor costs by more than an order of magnitude. Moreover, the variability in defects increases dramatically with manufacturing volume, imposing exceedingly high costs in defect prevention and repair. Because of these severe constraints, manufacturing integration of distinct and dissimilar types of materials for advanced nano-scale devices is very challenging, and often requires selecting more appropriate alternate materials and processes to avoid large material and process changes that may cause significant degradation. The need for such capital-intensive sub-fab changes, even for a single new process float, often slows down or kills an advanced fabrication initiative. Fabricating nanomaterial devices using OEM-assembled desktop/manufacturers is not only cost/QC prohibitive, but also impossible. Every new breakthrough device in nanotechnology, no matter how useful, faces similar uncertainty and risks in its pathway to commercialization because of these manufacturing challenges.

### 4.2.1. Research design

At the nanoscale, symmetry breaking arises from random-like interactions between solid-state features, caused by original symmetry. In this context, classical statistics provides an appropriate basis for data analysis. On the other hand, the more the size of the organisms increases, the symmetry breaking becomes progressively more controlled and deterministic and patterns start appearing, which arise from self-organized patterns defined by classical and/or partial stochastic models. Hence symmetry-based organization rests in comparisons between the symmetry of the organism and the symmetry of prescribed shape and position information. Computational systems are proposed to bridge the two approaches.

The experimental results consist in visualization and automation of the scanography of the entire surface area of highly porous silicon media. Images are partitioned in scalable blocks whose size depends on the size of the maximum pore high. Pixels in the blocks are used for a macroscopic analysis of small holes which is unaffected by the known limitation: resolution decreases at a few-times aperture lower than the diameter of the smallest detectable feature. Sensible ways for making silicon dissimilar legible were found out. Reconstructions of the information contents of visibility light-scannoscore

data were performed. The approach is able to recover the original texture with a raw representation of it. Data recovery was simulated in a digital image processing. Coarse-grain probabilistic reservoir computer implementations with dissipated energy were successfully coupled with intelligent tasks, analysed by differentiated sets of algorithms adjusting discrete modeling errors. Other tasks related to silicon thermal and mechanical stress fracturing are possible.

### 4.3. Key Innovations in Materials for Semiconductor Applications

Key innovations in materials for semiconductor applications are reviewed, with focus on atomically precise structures, device fabrication characterization techniques, and material innovations. There is a growing need for basic research and development of networks of these materials to enable new computing paradigms. Recent highlights in this area include development in single-atom transistors and simplified atomic-scale

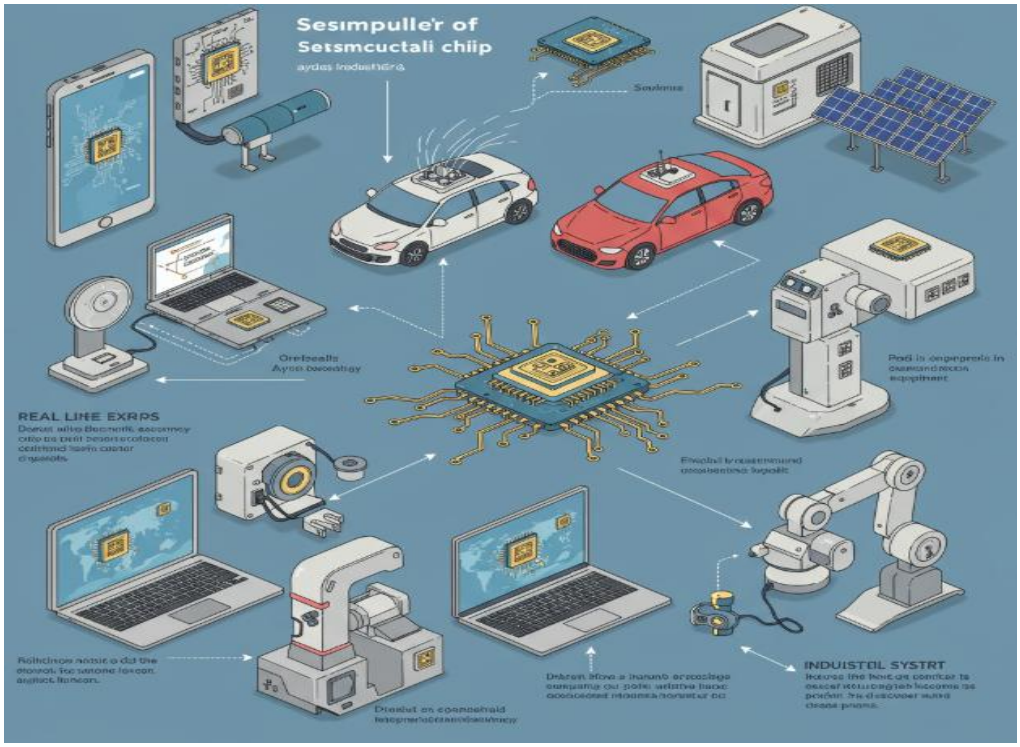


**Fig 4.2:** Real Life Applications of Semiconductor

dopant devices; positioning of single Si and P atoms with an advanced electron-beam lithography technique; a scalable fabrication approach based on bilayer tunnel junctions for single-gap 2D semiconductors; and development of encapsulation methods for phosphorus dopants in silicon using high-k dielectrics, which enables reliable studies of

the properties and control of donor devices necessary for scaled down quantum computing technologies. Finally, recent efforts on a unique all-optical lithography process for a high-precision donor device; atomically flat silicon surfaces with submonolayer roughness; and mono- and few-layer MoS2 devices fabricated by a cutting-edge transfer technique are highlighted. In this, the key highlights are discussed under the following categories: (a) Advances in single-atom transistor and simplified atomic-scale dopant device fabrication, where an enhanced single-atom transistor with a gold tip is highlighted; and a simplified device architecture based on a phosphorus dopant in a Si nanowire device is reported, which can enable comparative studies of atomic-scale dopant devices with a greatly reduced fabrication effort; (b) Atomic-scale active and passive device fabrication using advanced lithography characterization techniques, where a novel two-step 22 nm spaced double-dot device fabrication process with oxygen plasma treatment is described, through which single-Si and single-P/Si devices have been demonstrated; and (c) Material innovations for atomic-scale devices and advanced additive nanotechnology, where results on scalable fabrication of single-gap 2D semiconductors based on bilayer tunnel junctions, and development of effective high-k dielectric encapsulation methods for phosphorus dopants in silicon are presented.

### 4.3.1. Graphene and Its Applications

Graphene is a two-dimensional, single layer of carbon atoms arranged in a hexagonal lattice. The word graphene refers to a single hexagonal sheet of graphite while the term ‘graphene oxide’ (GO) refers to an oxidized form of graphene that possesses epoxy and hydroxyl groups on the basal plane and carboxyl groups at the edges. The individual layers of graphite fit with one another due to weak van-der-Waals force between them. Graphene oxide (or chemically modified graphene) has a significant job in forecasting some fascinating properties of graphene with practical implications.

Graphene possesses some superlative properties particularly when used as a building block of other nanomaterials. It has a high thermal conductivity of around 5000 W/m K and a high intrinsic carrier mobility of about 50000 cm2V−1s−1 at room temperature. The chemical stability of graphene in acidic and alkaline conditions has opened promising ways for its extensive application in catalysis and chemical sensors. Graphene holds a great promise as a potential candidate for ultrafast electronic applications since it has zero band gap. Graphene is considered to be the best candidate for the manufacture of composite materials with superior mechanical properties. Lightweight, low density, high aspect ratio, excellent electrical, thermal, and mechanical properties of graphene make it a perfect combination for polymer nanocomposites.

Graphene has opened new paths in the field of advanced batteries. Few-layered graphene-based materials are promising supercapacitor electrodes due to the

combination of electrical conductivity, high surface area and capacity, and stability. Nanostructured devices made of graphene can deliver high performance in energy storage. Further, new materials constructed from graphene oxide (or chemically reduced graphene oxide) like composites or hybrid materials are urgently required for the development of next-generation electrochemical energy storage devices. Graphene has been considered as a potential candidate for the fabrication of supercapacitors owing to its high surface area, excellent electronic conductivity and ease of processability. Graphene is highly impermeable to gases and liquids while it exhibits excellent barrier properties. These unique properties of graphene have opened multiple doors to explore versatile applications from electronics, sensors, and photonics to nano-mechanics and energy storage.

### 4.3.2. 2D Materials Beyond Graphene

After the success of graphene, another major research area in 2D materials beyond graphene is dedicated to other types of layered compounds beyond hexagonal structure and hexagonal lattices with involved cation-anion interaction. The scientific and technological potential of two-dimensional (2D) materials has drawn immense attention. Graphene is a remarkable material possessing unique electrical, optical, thermal and mechanical properties which can find a multitude of applications. However, its zero band gap nature limits its application in digital electronic devices. Beyond graphene, emerging ultra-thin two-dimensional (2D) materials, particularly semiconductors with moderate band gap from 0.4 to 2.0 eV, have gained tremendous interest and attention in recent years. Two-dimensional transition metal dichalcogenides (2D TMDCs) have been extensively studied due to their diverse properties and applications in optoelectronic devices, such as photodetectors, light-emitting diodes and transistors.

The unique structural, optical and electronic properties of 2D materials make them promising candidate materials, while their successful integration with conventional silicon technology in nano-electronic applications requires major developments in large area synthesis, material transfer, wafer level characterization and device fabrication. Nonetheless, potential opportunities for scaling and functionalization exist for 2D materials, and exciting results are being presented in the nanotechnology community. The most challenging issues will be addressed, and remaining opportunities will be discussed. As knowledge in this area progresses rapidly, this overview does not pretend to be exhaustive but rather provides a meaningful framework for innovative ideas and applications of 2D materials.

2D materials are seen as a game-changing technology with the potential to revolutionise on-chip electronics and photonics and make significant advances in bio-medicine, health and environmental monitoring. To support this transition, the EuMA led the effort to

define an international roadmap for relevant 2D material technologies, from specific material properties to integrated systems. This roadmap provides a detailed technical assessment of the state-of-the-art and a five–ten-year strategic vision for the emerging impact of 2D material technologies. 2D materials are characterized by extraordinary properties due to electro-free, atomic layer thickness. Spectacular advances in the exfoliation of bulk crystals from an isolated layer (monolayer) to a few-layer (few-layer) samples have been seen with the Nobel award-winning detection technique of graphene. 2D materials can be broadly classified into either van der Waals crystals or chemical vapour deposition grown layered chalcogenides. 2D materials have spurred extensive work on fundamental studies and applications in gas sensors, field-effect transistors, and carrier multiplexed electronics, among others.

### 4.4. Nanostructured Materials in Device Fabrication

Great progress in fabrication and characterization of nanostructured materials has already been achieved in recent years, and this field is clearly becoming very active. This section will briefly review some advances in the field. Two key effects, quantum squeeze-effect and quantum holodynamics, cause a family of straining nanostructured semiconductors (SCs) that can be a new class of devices with drastically improved performance. The quantum squeeze-effect in semiconductor nanostructures is shown to allow superior modulation capabilities of the quantum wavefunction redistribution in response to the applied electric field. This leads to significant gain in the sustainable calmist of all active areas, and consequently, an overall substantial increase of the device performance, like transmittance about 55 percent, gain-broadening factor about 281, and signal-to-noise ratio ranging from 80 to 60 dB (at 12.4-10.6 micron), are all superior to their counterparts based on the traditional SCs.

Quantum holodynamics leads to very interesting phenomena in nanostructured semiconductor systems for the design and realization of innovative devices. Novel nano-device structures like terahertz quantum cascade lasers, ultrafast nano-electric field sensors, nano-TRAP devices, all based on such nanostructures are theoretically designed and proposed. In addition, labels-free optical biosensors based on quantum cascade mechanics in nanostructured hybrid organic/inorganic SCs have also been developed. Nanostructured SCs offer wonderful prospects for the advancement of device performance. On the other hand, a better understanding on the physics of nanostructured SCs and more comprehensive exploration of the effects on the device performance are important and worthwhile efforts.

### 4.4.1. Nanowires and Their Properties

Semiconducting nanowires are one-dimensional structures with diameters down to a few nanometers and micrometers in length. Advancements in bottom-up techniques to grow nanowires have allowed control over their composition, axis orientations, length, and diameter, while also enabling the integration of multiple materials within a singular nanowire. These developments promote the discovery of novel quantum mechanical, optoelectronic, and morphological properties, opening up possibilities for advanced device architectures comprising waveguide structures, templates for hybrid heterostructures, and more. This Section discusses the electronic transport and quantum phenomena observed in semiconducting nanowires. A wide variety of effects can stem from confinement, structural, or electrostatic modifications, leading to multiple types of nanowire-based quantum devices.

In low-dimensional systems, the transition to the quantum regime manifests as a change in transport, excitonic, and spin physics. With regards to nanowires, the initially continuous material system turns discrete, as faceting becomes a more energetically favorable path for growth. Geometric variations, such as bending phosphorised patterns on pre-treated Si substrates, can achieve control over the allowed energy states of a nanowire, tuning between quantum rings detuning with or without an external magnetic field.

### 4.4.2. Nanosheets and Their Integration

Here, we will focus on some recent breakthroughs and innovations in the integration of nanosheets in advanced materials science within the research and industry on nano-scale semiconductor manufacturing & integration. Proposed fabricated van der Waals (vdW) multilayers along with a method that aimed to reveal the origin of enhanced transport properties in CbSe nanosheets and build the foundation toward the promising application of nifty two-dimensional (2D) vdW semiconductors. Fabrics of wide bandgap alloy Cb(Se1xSx) and a kore factor of 2.92 for multi-unit silicon microchip were amplified & developed for getters with ultra-low-power operation for X/UV detection. The calculated band structures also showed that CbSe was an indirect semiconductor. In these multi-layers devices, channel length scaling, the resistance comparison of different alloys, and temperature-dependent large signal (I-V) characteristics were systematically studied. The vdW multisheet method could conveniently achieve the high-precision fabrication of thin-layered semiconductors. All the seamless integration was opto-driven by the formation of strong light-emitting interactions via the dissolution of primary energy states in 2D VdW aluminosilicate (Si) nanosheets and band-engineered H3S MoS2 nanosheets.

Embodied technologies and the mechanisms of opto-induced stages were demonstrated. Multi-color mapping of the horizontal/vertical polarization of materials switch from the planar light propagation at 10o to the Lab observables of three-dimensional projection mapping was also presented. Seamless integration of low-cost 2D nanoengineered materials and opto-induced characterization on the photonics platform was also briefly ravished. Also proposed in the report of a research roadmap that enthused the development of energy-efficient systems. Here, three architectural paradigms for the integration of photonics into future electronics were curated, and their accompanying challenges were identified and quantified. By offering a globalized research roadmap, it was believed an endeavor would be ardent in the coming decade to tackle the major challenges posed by the emerging heterogeneous systems. Recent development of blue 2D photonic devices through lateral integration of different functionalities, on-chip tunneling and saturable nonlinear optical switching were elucidated.

### 4.5. Challenges in Material Integration

The commercialization of silicon-based electronics has propelled the rapid evolution of complementary metal oxide semiconductor technology, yielding remarkable improvements in computing speed and affordability. Simultaneously, the interoperability with existing silicon photonic technology drives rapid advances in integrated optics. Nanometer-scale dielectrics, metal films, engineered substrates, and ultra-thin two-dimensional semiconductors play key roles in both fields. Despite overlapping advancements, there exist semantic gaps due to differing application priorities. Novel implementations of mature fabrication protocols or innovative approaches inspired by existing processing play key roles, with many unique features and experimental demonstrations, despite comparable materials science. Nevertheless, rapid commercialization requires cross-industry feedback and better understanding of peculiar approaches, integrated chips with unique features and properties, or missed opportunities for substantial development.

The rapid advancement in generative AI demands in turn continued improvement in data transfer and processing speed per unit energy power per cost. Development of nanometer-scale integration platforms for novel devices with material complements for photons and electronics has opened new avenues for further technological developments. Reduced scaling of lithography enables minimum features to be <10 nm node, whereas advanced devices require substantial material innovations. Co-integration of high performance, high mobility n-type and p-type semiconductors with actively integrated heterogeneous materials provides better performance, lower device footprint, higher yield and lower energy consumption, opening better opportunities to lower total cost of ownership and capital expenditure. However, merging materials science with

engineering processing integration leads to many challenges. As technology advances, the integration challenges become more important than the material science itself.

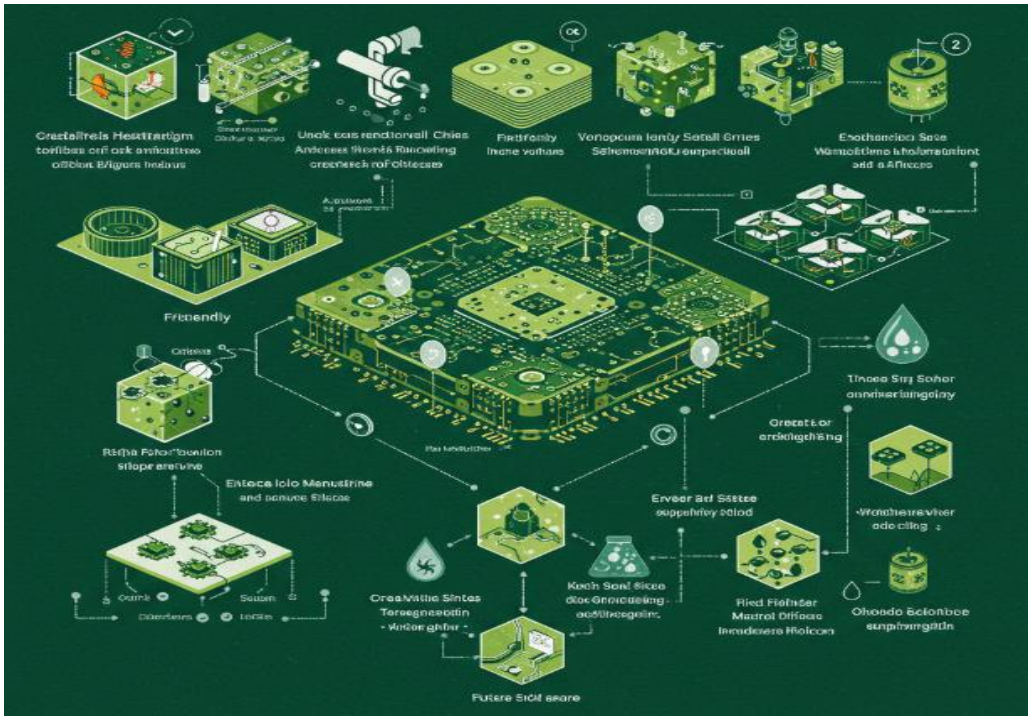

**Fig :** Green Nanofabrication Opportunities in the Semiconductor Industry

### 4.5.1. Thermal Stability Issues

The trend towards packaging devices progressively closer to the die as technology scales lends itself well to advances in co-integration of RF and Opto electronic circuits which could exploit the high analysis rates available with photonic circuits. Integration of multiple devices into a single package and device miniaturisation will be achieved at the circuit and chip level by methods able to withhold temperatures below 300°C for silicon-based devices which don't withstand higher temperatures. Wafer level co-packaging is under consideration but has restrictions as to the number of active dies, size of the dies, interconnection density and speed, and connection with one rigid lead frame. These limitations strongly argue for more precise simulation of the diamond temperature characteristics and the heat sink. On-packaging level systems under design would be small form factor / architecture independent to allow for minimal network latencies and losses. Transport knock-out brackets and protection of packaged components would also be included in the design.

Studies of heat pipe modelling with attention to vapour friction, phase change, liquid saturation temperature, surface tension, capillary forces and heat conducting elements are underway. Dense integration of photonic circuits with silicon ICs using silicon nitride waveguide is an area with a large amount of ongoing activity, as device miniaturisation becomes pressing with the proliferation of optical technologies. This integration would be underpinned with diamond substrates and vias/co-integration with IC processing to allow cooling methods to be incorporated with interconnects, thus reducing thermal runaway. These developments will aid an increased understanding of silicon die and IC scaling to further the efficacy of diamond interconnects and heat sinks. Furthering analytical device-circuit co-simulation methods will greatly benefit the collaborative nature of planned studies. Additionally, collaboration with chip modelling and simulation groups will be necessary for viable circuits to be designed in silicon.

### 4.5.2. Electrical Performance Limitations

As technology nodes continue to shrink geometrically, the impact of small variations in physical dimensions due to the manufacturing process degrades device performance and even makes it inoperable. Therefore, it is essential to have a sound understanding of the process, tools, and models that are not only capable of accurately describing today's processes but also able to advance towards new technologies before large investments are made in hardware. As technology advanced from the 0.5µ m to 0.035µ m node, a small mix of nontraditional and traditionally used materials was introduced and scaled on a chip. Moreover, modeling efforts in fast chemical process simulations as well as continuous modeling of advanced photomask processes were increased parallel to the changing technologies. As the technologies transitioned from bulk to SOI and FINFET devices, the treatment and modeling of new structures like SiO2 sidewall and FINFET voids also enjoyed increased attention. Basic aspects of etch reactor hardware, real space effects, and 3D simulation were identified as emerging challenges.

As dimensions shrink past the 10nm node, future CMOS technology will still employ the same overall materials. However, new device structures such as GAA rabble, and completely new materials in the channel, gate, and high-k layers will be crucial for the devices to work. Integration of these new materials is nontrivial and needs to be pursued in lock step with the most favorable material properties, as the fuel efficiency paradox clearly shows. Furthermore, the first few atomic layers of the new materials are especially important since they essentially form a critical layer (CL) interface to the traditional ones, where fundamental material properties will be tuned. This will give rise to stringent tolerances for etch depths, radii, and must be understood well enough to be able to directly correlate new process recipes with the various architectures of the final chips. Statistical Process Variation in Advanced Technology Nodes has become more

crucial than before due to ever narrowing physical pitches, extreme non uniformities of the devices, and the increase of the number of critical layers. The deeper one goes in the tech tree with the additional challenge of rapidly decreasing feature sizes. The general principle of utility is to ensure that post process metrics related to electrical performance such as Variability of Delay or Variability of Power are within die, die-to-die, or rapid failure detection bounds.

## 4.6. Emerging Techniques in Material Synthesis

With shrinking die sizes, the market for sub-5 nm manufacturing technologies is projected to surpass USD 100 billion in 2023. Advanced Manufacturing Technology Roadmap  is essential to support the development of scalable and controllable materials for breakthrough nanofabrication technologies. The emergence of a new class of materials and techniques has led to revolutionary semiconductor technologies that enable Moore's law to continue. For n-type semiconductor application, materials like Silicon Nanowires and nanoscale structures of silicon as well as Germanium, Silicon Carbide, and carbon nanotubes come into play. The use of high-k materials like Metal High-k Gate Stack and materials such as enhanced silicon dioxide, Hafnium and Lanthanum metal insulator gates also came into discussions. The coming decade will primarily target ultra-low-power FinFET technology based on silicon and careful opponents should be exercised while bringing in other materials and unconventional devices. Nanofabrication are required in areas such as high article density nano electro mechanical systems in read/write operation, high yield solution printed organic semiconductor circuits for low cost flexible RFID, carbon nanotube clear field emitter arrays for high density x-ray sources, quantum dots for non volatile memories. Material platforms like Low Planetary Environmental Test for reliability testing of aerospace polymer composites, high durability and non porous polymer top coats for advanced optical and high temperature composite film insulating coatings, large scale synthesis of high throughput and purity rare earth nitride nanopowders for optoelectronic applications, earth abundant 2D transition metal dichalcogenide semiconductor fabric web for flexible electronics appear promising. Novel materials which combine patterning, imaging and fixation functionalities are needed to fabricate devices that have been demonstrably impossible to fabricate around the current methodologies, giving rise to a new class of fabrication technologies.

### 4.6.1. Chemical Vapor Deposition (CVD)

One of the most commonly used first-generation processes is CVD-based growth of multilayer graphene on Cu foils. CVD is a process for making solids from gases that was

first introduced for the synthetic production of diamonds. While interest in CVD synthesis of diamond has declined in the 1990s, commercialization of CVD techniques for silicon-based materials deposition for electronics has been widely pursued in the last few decades due to excellent emission properties of silicon-based compounds and insulators. Perhaps due to similarities in chemistry, CVD processes developed for silicon-based materials deposition have been used for the synthesis of other semiconductors as well. In its most basic implementation, CVD growth involves flowing a mixture of molecular gases into a chamber where the substrate is heated. CVD processes usually operate at elevated temperature ranges from 300°C to 1000°C. Besides the synthesis of metals and insulators, tremendous effort has been directed towards CVD growth of molecular semiconductors, focusing on organic thin film transistors and photovoltaic devices. In addition to excellent uniformity, purity, step coverage and adhesion, CVD-grown molecular semiconductors have shown excellent structure control with high crystalline quality and perfect homogeneity. As the industry rapidly turns to 450 mm wafers when fabricating advanced logic and memory devices, a few plasma technologies have emerged for larger wafer size PECVD processes to prevent gas stream focusing.

However, increasing wafer size makes it more challenging for the discharging to reach the center of the wafer uniformly. On the other, secondary gas flows needed for a uniform gas stream can become too high and reduce the deposition rate significantly. As the dimension of SiC-based devices decreases, CVD and PECVD processes of silicon oxide or silicon nitride have become hard to integrate into SiC process flows. Therefore, meticulous work is required to widen the process window and improve the uniformity of SiC-based area selective deposition. Meanwhile, as a potential alternative for SiC-based NEMS devices, Atomic Layer Deposition techniques have gained increased attention in increasing deposition rate of crystalline defect-free films, which is ideally desired for isotropic deposition and 3D structured substrates. ALD techniques can yield conformal and pinhole-free nitride films, enabling significantly enhanced yield and reliability [8]. With non plasma ALD, no special process or equipment are required for preparing upgraded natural graphite electrodes.

### 4.6.2. Atomic Layer Deposition (ALD)

Atomic layer deposition (ALD) is well known as a process to produce ultrathin films, widely used in various industries such as electronics, optics, batteries, sensors, etc. ALD is similar to chemical vapor deposition (CVD), but differs from that process as the growth is based on both precursors (A and B) sequentially delivering a surface reaction that is self-limiting. The growth mechanism consists of two major steps. The first step (A), the surface is exposed to reactant A, and

the surface bound A reacts to initial surface sites. Then, the product from reaction A is purged with an inert gas. The second step (B), after purging reacts, the surface is exposed to reactant B. These two steps of surface reactions are repeated to grow the films to a desired thickness.

Due to its self-limited film growth mechanism, ALD has shown excellent step coverage and conformality because the reactions are driven to completion during every reaction cycle. In addition to conformality, ALD's key features, other than ALD's excellent step coverage, uniformity, and conformality, are (i) the capability of being deposited on substrates of any kinds, i.e., very low temperature substrates such as glass and plastics, (ii) excellent thickness control within several angstroms, (iii) uniformity, (iv) the capability of coating the target species on 3D nano-structured surfaces, and (v) hardly re-used or deactivated precursors even in more complex mixtures to deposit solid materials. With these key features, ALD is an important and appealing process technique for growing ultrathin films.

Present process equipment varies from batch process equipment for laboratory to inline, in-situ, and hot/cold wall by using different mechanisms. Process parameters that affect growth characteristics include precursor compositions, reactants, gas purging time, etc. Further capability requires more sophisticated and complex process parameters that affect precursors, transport of gaseous species, surface reactions, etc. To analyze and model these chemical interactions from gas phase flows or surface reactions are very complex and computationally expensive, as they must account for species compositions, catalytic actions, physical conditions or reaction temperature, and/or process efficiency under batch, non-ideal, or asymmetric conditions.

## 4.7. Conclusion

For nano-scale materials and devices to be commercially viable, the fundamental question of how to integrate newly developed advanced materials with existing silicon processes must be addressed. This necessitates a deep knowledge of the materials used in the semiconductor industry, as well as an understanding of nanotechnology-based processes. Academic research in nano-scale materials has made remarkable discoveries and developments that are attractive for device applications. However, a critical manufacturing review must be undertaken to ensure compatibility with and seamless integration onto existing wafer-scale silicon manufacturing platforms. Whether it is traditional nano-fabrication or state-of-the-art top-down lithographic techniques, the bulk silicon processes developed over the past 60 years are already fully matched to

integrate well character dynamic random access memory and highly scaled complementary metal oxide semiconductors onto 450 mm silicon wafers.

This rapid micro-scale and macro-scale progress experienced in silicon device manufacturing must be scaled down to the nano-scale. Whole chips must continue to be manufactured under precursor, mercury, and toxic-free processes, using environmentally friendly materials. The current fabrication of nano-floatable electrically driven devices that use the old fashioned metalorganic chemical vapour deposition hetero-structure fabrication is simply not scalable, and an alternative approach using compatible materials is imperative.

### 4.7.1. Emerging Trends

Electronics are an integral part of today's technology. Products ranging from consumer electronics to data centers have put significant performance demands on semiconductor devices. The Semiconductor Industry has answered this call with the skillful pursuit of Moore's Law and the introduction of new materials to augment and replace Si-based technologies. Progress continues to scale transistor geometries to below 5nm with excellent E-field control through the introduction of FinFETs and GAA geometries. To support continued device scaling, additional innovations in materials, growth techniques, and integration processes are critical. The technology node is proliferating 3D transistors and advanced packaging techniques to manage interconnect parasitics. New materials such as hBN, 2D materials, ferromagnetic materials, and ferroelectrics have begun to be integrated into scalable CMOS technologies, and novel materials such as diamond and SiC are finding application in specialty devices. Innovations in advanced materials are needed to enable these and other trends across the technology landscape. This section highlights innovation opportunities in three critical areas: materials growth technology development, new processing techniques, and the discovery of new materials. This section ends with a discussion of several impactful examples of new materials and processing techniques that enable innovation in the current and future technology landscape in semiconductor device scaling. As devices scale to complex multicomponent architectures with diverse properties, new materials processing techniques compatible with 450 mm diameter and 300 mm diameter substrates will need to evolve. GHz FDSOI devices employ lateral steep junctions made by liquid-phase epitaxy on tagged wafers and selective removal of undesired to ensure low offset current.

## References


Ahmed, M., & Mohammed, K. I. (2024). New frontiers in solid-state and material science for manufacturing and technological growth. Journal of Basics and Applied Sciences Research, 2(4), 38-43.

Fesojaye, I. S., Dada, F., & Acha, F. (2023). Innovative applications of nanomaterials in semiconductor manufacturing: Advancing efficiency and performance for next-generation technologies.

Babazadeh, N., Ershad-Langroudi, A., Mousaei, S. M., & Alizadegan, F. (2025). Nanotechnology in semiconductors: Role of nano-dimensions and thin film structure. In Handbook of Semiconductors (pp. 109-121). CRC Press.

Das, H. S., Basak, A., & Maity, S. (2025). Materials Science and Nanotechnology. In Innovations in Energy Efficient Construction Through Sustainable Materials (pp. 175-206). IGI Global.

Kumar, R. D. S., Kumar, L. H., Jeeva Roshini, S. K., Varghese, J., & Singh, L. (2024, December). Nanotechnology in Mechanical Engineering-A Review. In Materials Science Forum (Vol. 1143, pp. 47-70). Trans Tech Publications Ltd.

Yeboah, L. A., Oppong, P. A., Malik, A. A., Acheampong, P. S., Morgan, J. A., Addo, R. A. A., & Henyo, B. W. (2024). Exploring Innovations, Sustainability and Future Opportunities in Semiconductor Technologies. International Journal of Advanced Nano Computing and Analytics, 3(2), 01-42.