Deep Science Publishing
https://doi.org/10.70593/978-93-49910-47-8_9

DeepScience
Open Access Books

Chapter 9: Testing, verification, and quality assurance in the life cycle of semiconductor product development

9.1 Introduction to Semiconductor Product Development

Microelectronics is one of the very high-tech industrial sectors, and its continuous growth and its influence on the evolution and development of digital life can be taken as evidence that such a statement is true. In fact, in today's world, ICs are found everywhere, ranging from cheap everyday consumer products to sophisticated, expensive, and complex military or aircraft devices. Nevertheless, all these products are required to be within an appropriate quality range. Most of them have several quality requirements, and quality cannot be verified without tests. ICs, chips, and semiconductor products in general must execute some tests before entering the packaging or post-packaging stage. Furthermore, testing failures cannot be handled unless somehow traced back to its cause. In order to improve the test capability, failures must be recorded and their diagnosis performed by appropriate means (Cabanes et al., 2021; Sundaram & Zeid, 2023; Hii et al., 2024).

When considering the life cycle of a semiconductor product, from its conception to the test along time to the disposal, most key and critical steps are performed in silicon; the most relevant design and characterization tools are implemented on the same platform. In the first place, design tools generate the necessary information to fabricate the product. Near-fabrication tools are better suited to enhance yield and controllability of the steps. In-process and post-fabrication test and quality verification tools are similarly implemented on silicon and do not need any additional hardware. The implementation of tape-out test and product-level diagnosis on silicon is not yet possible, though, and needle test hardware must be used. Good solutions from all these industrial domains involve large investments, and this is the reason why there are mismatches among tools

from different domains. Thus, tools should detect as many defects as possible and reveal candidate types of defects to limit the necessary test enhancement efforts.

Testing and Verification methodologies undergo fundamental changes with the integrated circuit becoming System on a Chip. System testing involves functional and structural testing of the IC, special attention shall be paid for fault detection and localization ability of the devised tests. A rapid test development methodology scaling down to higher performance digital mixed signal very large scale integrated device input-output macro models verification with analog delay modeling is in practice using numerous ICs and their parameters from design environments. Testability and fault management aspects of the design shall be looked into by identifying the need for the development of larger heterogeneous memory testing at system speed (True et al., 2021; Zheng et al., 2021; Zhou et al., 2022).

Fig 9.1 : Test Quality In Semiconductor Devices.

9.1.1. Background and Significance

The quest for increased performance and reduced cost-topology optimization of product design as the primary area of research in semiconductors over a long time has now transformed into "International Industry Standard Low Cost Reliability." The semiconductor industry could not escape from this transformation, particularly in the VLSI devices where million to billion small devices are integrated on a single chip. The semiconductor product market is a low-cost market, and this could be achieved only by a large degree of circuit integration. Also, the technology is continually changing to overcome product demand by stacking more devices and interconnections. Test and quality assurance for the newly formed product and continuously for processed chips are crucial in this transformation. The testing and verification techniques which are in use today, both for pre silicon and post silicon verification need to go through rapid newer development and optimization methodologies keeping product cost low and detect a defect in the silicon below the threshold level.

Market pressure and increased demand for high performance consumer electronics today compelled the semiconductor industry to continuously scale down to newer and smaller devices. The newer designs, technologies, market-driven, chip grading complexity, and competitive lead-trial and debug patterns with reduced cost need to be developed. In this research, system testing and post-silicon verification techniques are kept in focus.

9.2. Overview of Testing Methodologies

The IC is densely packed with several thousand gate levels, and with the advent of IP cores comes the challenge of testing a chip with several million gates in a few hours and with >99.99% fault coverage. The IC design is done using a hardware design language. The RTL (register transfer level) description should undergo various checks before entering the synthesis tool. The checks performed in HDL design are logical simulation, equivalence checking, formal verification, DRC (design rule check), and parasitic extraction simulation. Then the various data generated in the above steps are handed over to place and routed the chip layout tools via the floor planning. In conjunction, the chip layout designs are checked with layout versus schematic (LVS) checks. LVS checking is done in several stages: contact level, layer level, and top-level checking. After fabrication, the chips will undergo probe testing for processing defects, and all the chips that pass the test will be sent for packing. The assembly will be placed in chip carriers, and the BGA and QFPs will be/are tested on wafer probes and complete packaged ICs using the automated testers.

The following steps are involved in this process: probe card design for some carrier types, external circuitry or test hardware design, implementation, and validation. GPU

handles the die-level plan check, netlist checking, probe coverage check, pad-to-die and die-to-die pad alignment validation, and pad, etc., electrical rule checks (ERC). Chip-pin to card-pin check and wide-angle view image generation are possible . The objective is to validate overall performance of the tester hardware before loading in the tester, and once this is completed, it can be delivered for identification of blended parts. This step will capture the non-IDC quality variations in IC tested at different ends. The failure analysis will be pointed to the probing level via WCP and CT and soaking before the final report.

9.2.1. Functional Testing

Functional testing is performed to verify that the developed chip meets its specifications. Each chip is examined to determine if it implements the intended function correctly. To ensure functional testability, test conditions must be set during the product design phase, including design for test improvements. In particular, embedded memory devices are dedicated components that are mostly deployed in modern system-on-chip devices due to their low area consumption and power demand advantages. At the same time, they represent a great challenge for test engineers since they cannot be accessed directly by external test access mechanisms or scan chains, so the physical test vector generation must be done at a higher level in terms of representation using generic digital, analog or mixed signal functional test injectors/extractors.

One of the first tests performed on a chip is the functional test. This ensures that the logical generic functionality of the chip is in accordance with the design specification. A good functional test should cover all paths in the logic to screen out speed and design errors. The aim is to test that the design performs the desired function thoroughly. The test consists of different phases such as vector generation, fault simulation, fault grading, untestability analysis, test reduction and test programming.

Functional tests for RF and microwave are usually performed in two test stages: first, a wideband calibration test is performed by a full-parameter vector network analyzer to separate quickly the good from faulty ICs and then a focused and precise, narrow-band functional test is selectively performed with a more expensive, narrower-band multi-port vector signal generator vector signal analyzer. The RF properties on-chip measurement of most of the RF-to-bitmap IC involves a two-step functional test hardware-software implementation. In the first step, each die of the wafer-under-test is cataloged by S-parameter full-parameter vector network analyzer measurements. Good and bad chips are separated by a scan loss calibrated lower threshold, greatly reducing the cost of testing chips in bulk. However, with some bad chips appearing normal at this point, a second more expensive based functional test is performed to measure the more complex sampling output bitmap functionality, ultimately aiming the detection of faulty chips.

9.2.2. Performance Testing

On-chip memory testing is important in system-on-chip (SoC) integration. After the test generation step, standard cell libraries, test vectors, and flip-flop descriptions are determined. This paper performs an analysis of memory-tester connection schemes based on multiplexed pins. The aim is to approach a setup that reduces the number of off-chip tester pins. Each memory cell is explained in detail, and the behavior of each output scheme is modeled for the simulator to generate the test. New result values are also generated with an associated fault model representative of the memory. The performance of the simulator and some simulation results are shown. This paper presents a mixed mode approach for testing a telecommunication chip integrating a low phase noise oscillator and a biphase modulator. The suitable measurement performed on the discrete components, such as jitter and voltage at node, is adapted to the IC step response. Test simulation runs are performed within the chip design framework to verify the proper translation.

All issues for on-chip testing of a 700 pS time interval resolution 10-bit pipeline ADC with switched-capacitor array are discussed. The impact of the active core and the amplifier design concept on the jitter specification of the ADC is analyzed. The traditional testing method for measuring SNR and INL with a random sampling source in an external benchtop setup is shown to be ineffective. This paper addresses design-for-test solutions in the analog circuit that incorporate a ring oscillator and a counter in conjunction with the Built-In Self-Test (BIST) approach. They leave the netlist of the core unchanged but add just a few off-chip redundancy circuits and FPGA logic to implement slow and fast BIST methodologies. Simulations have been performed successfully to check the acceptability of the methods and to understand the trade-offs related to yield.

DC-characterization and testing techniques together with the corresponding test devices are presented. The main objective is to assess device quality at wafer level as part of a production line. The device under test is an N-channel MOSFET. A test chip and a measurement module conduct automated DC-testing of devices on a wafer by a computer-controlled setup. Measurements include VTH determination, Id-Vg curve, and transconductance evaluation. The performance of the device is extracted from the results of the tests. In addition, a procedure is proposed for enhancing the testable chip area and avoiding defect-induced measurement errors.

It is possible to design and build fast, low-cost, effective built-in self-test (BIST) and built-in self-repair (BISR) circuits for embedded memory and logic devices. Standard factory test patterns designed for logic and memory are often inappropriate for the full speed, high density, power-efficient designs needed in cell phones, computers, and digital video. The creation and implementation of low-power, nonintrusive BIST and

BISR circuits requires a thorough understanding of memory technologies. In use, during functional mode and when the embedded device is turned off, digital BIST circuits can impact system performance and reduce power. Dynamic logic BIST must be gated on when memory cells are static. A variety of self-test and self-repair circuits must be described.

9.3. Verification Processes in Semiconductor Design

Functional verification is an essential step in every design development process to assure quality in the final product. However, the verification portion of every design development is the bottleneck in most of the design development which takes up 60% of the overall design development period. The design is normally verified by creating a functional model to stimulate its operation to check its correctness. Simulation will be run on the functional model for a set period using a set of input test patterns to ensure the design correctness. One of the key factors in slowing down the design verification flow is the long simulation time during the pre-silicon functional testing of the design. The long test simulation time issue is seen in NAND Intellectual Property pre-silicon validation. The simulation runs on a register transfer level model to check the IP's functional correctness, having a length of about 6 hours on average. However, the large test case numbers generated by the automatic test pattern generation tools require a simulation time longer than 7 hours to complete, which causes the failure of the validation test on the generic validation platform dedicated to the function and timing test of the IPs in the testing environment. To ensure success, this overload is unable to be accepted in the production testing.

In a word, verification is one of the major steps in the Integrated Circuit development flow. Besides the difficulties in testbench development, large verification effort, and lengthy verification time, there are numerous cases where the absence of verification planning leads to delays of tape-out where the ICs are sent to fabrication. All of these difficulties show the need for a verification methodology that can provide better verification productivity, coverage, and reusability to IC development companies. A verification methodology is needed which addresses key issues in providing a structured and efficient means of IC verification at all stages. Such a methodology will introduce a new hardware language procedural abstraction to design specification language in a similar way that the other standard hardware description languages enhanced. The verification methodology needs to provide an overall infrastructure for reusable verification. This infrastructure consists of the verification languages and documentation, and any support. Ultimately the methodology will enable engineers to apply similar techniques and to enhance the verification infrastructure as new methods evolve and are documented.

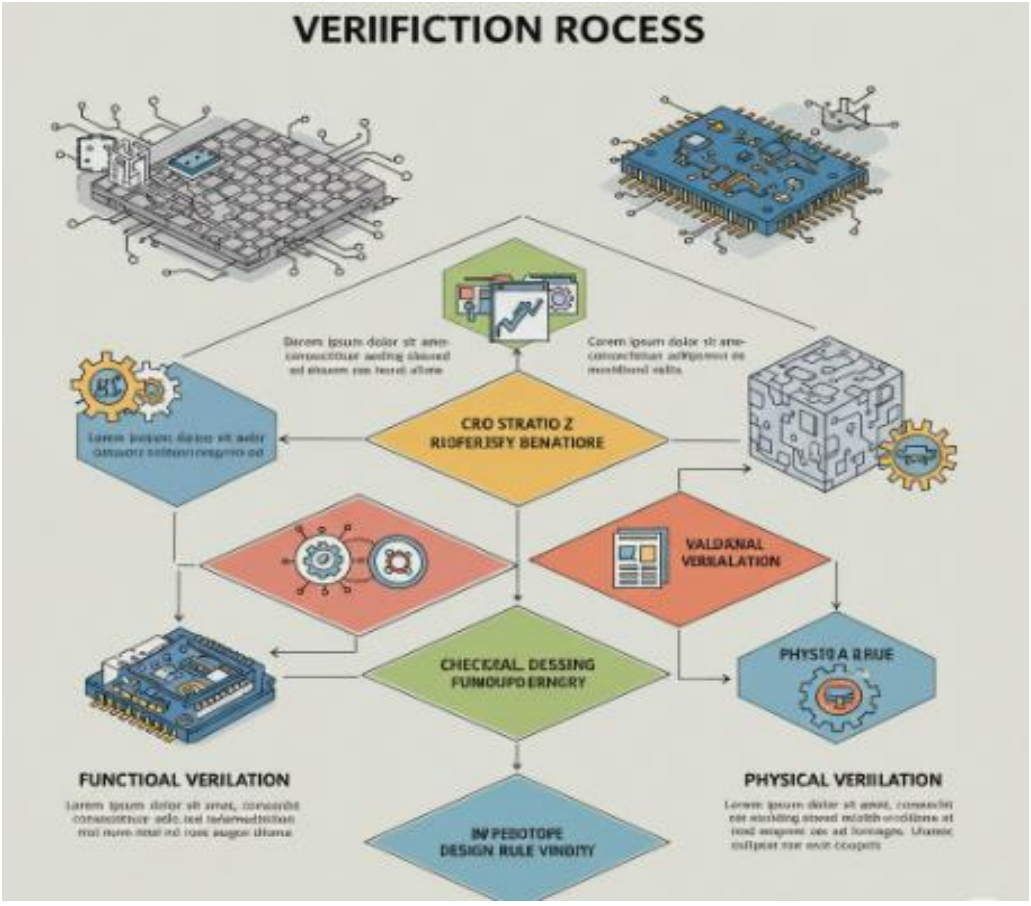

Fig 9.2: Verification Processes in Semiconductor Design.

Testing quality improvements together with design improvement measures are being pursued by IC manufacturers to enhance yield and reliability, while the need for faster testing and return on investment is pushing the limits of current test technologies. In the background of fast-changing IC technology, maturity testing, data mining, and software testing can be beneficial decision tools. On the one hand, mature manufacturing processes can be retained or maximized and excessive variations eliminated. On the other hand, circuit failure spectra can be mined to get insights into root causes of failures. These strategies improve testing efficiency and the reliability of products. However, there is little attempt to provide a guideline for planners of IC manufacturing tests. Wafer and package testing are the key phases which will be analyzed in detail. There has been a long-standing quest for faster and smaller testing equipment that preserves as much testing efficiency as possible. Design-for-testability improvement measures will also be reviewed since they need to be taken into account during the whole product drive phase.

Near-zero defect products are the constant pursuit of the semiconductor industry, and there are higher requirements for the safety and quality of automotive electronics. Semiconductor chips often use defect per million rate to indicate quality. Existing commercial automotive electronics support test repeatability. It is prudent to use repeat testing to select high-quality chips; otherwise, the number of chips with killing errors will increase, and vice versa. Using test repeatability can increase the number of high-quality chips that can be sold. In other words, the high market price causes increased quality testing effort, but the cost of test operation will be higher.

9.3.1. Design Verification

Verification is the process of checking whether a product has been implemented according to its prescribed specifications. In the design of integrated circuits, verification is about checking whether the actual netlist produced by the synthesis tools satisfies the actual HDL description and its formal specification. One approach to such verification is through simulations, where a simulator accepts the HDL description and a description of the test-bench (set of input signals), produces wave views, and checks its output against expected results. Although widely used, simulation-based verification is not exhaustive. To check any situation, potentially an infinite number of different input combinations may need to be tried in the test-case generation. Moreover, extracting the equivalent HDL code from the synthesized netlist remains an unresolved issue.

Designers usually create a smaller functional unit, write HDL code for it, which is then synthesized, checked again by simulators on RTL code, and handed over to a foundry for fabrication. Errors in HDL design that go undiscovered in the verification of HDL code can result in the fabrication of a final product with an unknown functional bug that may never be found. In ASIC design, the product development life cycle consists, in general, of design verification, physical design, physical verification, programming, testing, and packages assembly. Design verification is concerned with checking whether the HDL design fulfills the specifications. Testing is concerned with the linear circuit implementation checking whether the ASIC behaves according to specifications after fabrication. Both activities rely upon a combination of EDA tools that analyze the design operation and design test strategies.

9.3.2. Simulation Techniques

Simulation moves testing to a safe environment that does not risk physical damage to software or hardware under test. The lack of hardware error cases has motivated modeling faults in simulation. Injecting modeled physical faults into a simulation moves the error analysis to a safe environment. Imagine that the simulated hardware is

responsible for establishing a connection from a receiver to a transmitter. An error in the model causes it to reject all connection attempts, causing testing to fail. The hardware is not damaged - traces of its state during testing remain. This characteristic allows identifying and fixing the issue. In an injected simulation environment, triggering diagnosis is possible at the simulation level. Timed logs detail where in the simulation a junk value was produced. If this happens in physical hardware, no traces are left. The fault injection in simulation has reached a good level of maturity. Instructions on using fault-injection systems exist, offering automated document generation and a good debugging experience. However, there is currently no instruction manual on how to inject faults in simulation and debugging strategies. Opening the simulation environment to the outside world exposes the underlying implementation - there are many ways of breaking the model. Moreover, processing faults from live experiments in the simulation environment can lead to many questions during board auditing. Never before was so much information about the 4 M's of manufacturing accessible - something that could have led to dismissing octagonal chips in favor of more stable perfect chips.

9.4. Quality Assurance Frameworks

Here are a number of factors affecting the criticality of a semiconductor product. These include: a) Product specifications, b) Product target supply price, c) Product lifespan, d) Application life-cycle, e) Number, nature of key customers, f) Technology nodes, g) Test Mode, h) Dimension, and i) Geometry and external interface form factor.

(a) Product specifications: This is the most mature and certainly the most direct factor affecting product criticality in a semiconductor product. Product specifications encompass all the attributes needed by the customers to determine whether they would like to buy the product. Product specifications are the expectations of the product from the customers' point of view. Specifications can be at different levels of verifiability/quantification/measurement. For example, area, speed, power consumption, 1st die yield, long term reliability, etc., can all be quantitatively specified. On the other hand, robustness to noise, ability to deliver best in class power speed product, complexity of customer fine-tuning etc. are all difficult to specify but make a product very critical. Specifying the specifications, including the quantification of the specifications and determining the degree of criticality for each spec is often an undocumented but very important work flavor usually done in the design phase.

(b) Product target supply price: This is another very important and mature factor affecting product criticality. Products targeted for supply at very high prices are very critical typically for the design and manufacturing teams. On the other extreme, massively produced products that will not be sold beyond a certain price threshold are

mostly non-critical. Frequently, this is the major reason for not releasing or deploying a specified product.

(c) Product lifespan: This is part of the input product specification. The customer is expected to set products' expected lifetime, but this is rarely acted on by the engineering teams. Product lifetime is typically used as an input to failure analysis calculations. However, NMOS and PMOS, the 2 fundamental components for many ASICs, have different long-term life expectancies and are a good illustration of this input having very big ramifications. This is illustrative of how the final application often changes the nature of the very product itself sometimes in an unexpected way.

(d) Application life-cycle: Applications have lifecycles from initial coherent and exclusive hand-written applications to current diversity and multiplexing of a wide range of applications running simultaneously. Applications also evolve from "run and link" (one image early on) to sandboxed (next generation) to multi-application co-scheduling. Applications with more simple life-cycles are typically less paranoid.

(e) Number, nature of key customers: This item is a mix of pig-case (supply for the mass market of many customers is typically the least critical) and matured technology case (e.g. take a non-critical product, analyze its yield, noise, shape etc. and manufacture a better one at a smaller than its present size).

(f) Technology nodes: This factor affects quality assurance complexity and is usually a good indicator of product criticality.

(g) Test Mode: By far the best coverage is analog, but the other modes are fast catching up and being very widely used. By contrast, as more and more products have DFTs, this would become the worst in terms of product criticality, at least for New Product Ramp Phase where characterization is most vainly frothy.

(h) Dimension: 0.5 x 0.5 mm^2 devices and bigger ones are simpler and much easier to guarantee.

(i) Geometry and external interface form factor: This is often one of the biggest reasons for a product being critical.

9.4.1. Quality Control vs. Quality Assurance

Quality Control (QC) and Quality Assurance (QA) are terms frequently used interchangeably; however, both are distinct concepts in a Semiconductor Manufacturing Environment. QC focuses on the task of ensuring that product errors do not enter the assembly process, while QA focuses on ensuring that assembly defects never arise in the first place. To put it another way, QC is complaint-driven, while QA is preventive-driven

[6]. QC is the assessment of a product against a specified standard of desired characteristics by the end user. QA is the part of the quality system that evaluates product quality requirements, determining the activities needed to achieve that quality, and verifying that the needed efforts have been undertaken. Preventive QA activities are designed to include recommendations, training, and a checklist of construction details, while QC activities may offer spot checking, more extensive inspection, and quality evaluation measures. In Semiconductor Manufacturing this distinction is seen primarily in the different behavior of quality engineers and assembly supervisors. Not wanting to be seen as merely auditors, quality engineers want to go beyond complaint-driven control tasks to define assembly practice and enforce it. From this standpoint they have largely failed. Many engineers and managers claim that QA and QC are only as effective as the support they receive from management, and in one respect this is certainly the case. QC activity levels remain low because the level of complaints is low, not necessarily from a lack of Kalman filters. QA engineers, on the other hand, are viewed as little more than managers of training programs and trust in their process audits is low. But this sort of management is not a panacea; much more is needed. It is also essential that the right targets are selected to begin QA activity. Notions of a parity between preventive QA and complaint-driven QC reflect a failure to understand the nature of the assembly process and errors in a semiconductor design.

9.4.2. Standards and Compliance

Standards in the semiconductor industry mainly relate to long-term applicability and compatibility of products and equipment. On the product side, such standards are usually updated every three to five years. The most significant is the IEEE SEMI Standard 850, as it defines the test protocol for semiconductor products. These tests are performed with so-called test patterns in automatic test equipment (ATE), which execute a pre-defined sequence of tests.

The compliance tests will measure the changes in process, metrics, etc. of the devices and compare it with the baseline measurements done at the approval time at the foundries. If a data point exceeds the specification, a TDR (test data report) will be generated and sent to the design house. In the TDR, a comparison between the baseline and the current measurements will also be included, and the design house can obtain better insight into the product characteristics from the whole data set. Therefore a better understanding of the existing problems, and which corrective actions should be done, as outlined by.

Furthermore, along with the first-level device test, second-level measurements are necessary to verify how good the wafer test was. These measurements include scanning probe microscopy (SPM) and those tests are done at the packager level on a probe

station. However, it is essential to standardize how these tests are performed so that these second-level measurements can still be used as test data. Even with comprehensive standardization, it must be ensured that there will be a common understanding across companies.

9.5. Role of Testing in Different Phases of Development

In general, VVT becomes increasingly challenging towards the end of the development phases as design complexity increases and test time is limited. Companies face varying levels of test challenge depending on development phases. The incremental nature of learning and improvement of existing testing methods is often reflected in testing's evolution between product development phases. Importantly, invertibility of design integrity is provided from pre-production cleanroom to early production testing and finalize testing. Testing is less utilitarian than verification and thus more vulnerable to different perceptions. At the beginning of product phases (e.g. prior to the design freeze), testing can only validate design specification and early prototypes, but as designs mature (e.g. at the end of design and process qualifications), tests can be moved from production back towards engineering analysis. Often considered tedious and time-consuming, testing is nevertheless fundamentally an educative process in revealing design integrity and contribution to design improvement, delivery of better products and lessons for next generations.

Fig : Quality Assurance in Semiconductor Product Development.

Verification of designs covers a variety of activities including (1) design verification; (2) design qualification; (3) process qualification; (4) system qualification; and (5) product generation. Verification tends to become relatively easier and more certain towards the end of the development phases as designs become less variable and changed rates decline. The product is inspected and tested against design specifications, as well as assessed for ease of test generation and coverage of corner cases. It is ensured that existing tests handle all variations and conditions specified for parameter settings and operation platforms. Both test and redeem implementation are assessed for integrity with path coverage and excessive inclusions eliminated.

9.5.1. Pre-Production Testing

Pre-production tests should be considered an integral part of chip design, bringing a new way of thinking to chip-design teams. Issues strongly impacting the testability of any family of chips being designed need to be addressed at the specification stage. Specifications for testability in a large hardware design generally neglect the limitations imposed by structural partitioning on the test methodology. On a large or complex chip, aspects of design verification, validation, and testing impact the design flow. Emphasis is on pre-production testing and design issues that impact testability, capability, and procedures. These test-development issues are critical and yet often overlooked. Microprocessor memories are tested with a very fast signature-analysis technique long before chip fuses are programmed. Memory specialists believe eliminating memory tests does not reduce the intensive chip-design effort involved for unforeseen effects, nor is it a task that can be automated satisfactorily. The initiation for producing a new family of chips typically starts with the preparation of a design specification that addresses general function and performance issues. Designers and managers also must specify the automated-test-equipment environment in advance, including drivers, load board, temperature, and a-probe and/or view ports. Such specifications often do not discriminate between fabrication process styles. Specifying a completely different test methodology is risky, even for experienced chip fabrication and design engineers. The design teams have to stress-test the selected architectural approach with applications running in the vendor's worst-case speed and timing conditions and analyze the results for exactly the same operating speed or performance of the test. Most chip companies cannot afford expensive redundant parts or full test coverage. Test-development time and costs should be minimized by specifying the testing limits early. Testability is the first consideration; clearly, an "untestable" circuit design cannot be tested. However, spectacular test-factors improvements can be made through attention to testability down to the register-transfer level in the design verification, design division, and logic synthesis stages. Although not limited to scan options, design-testability enhancement has filter-vector-design implications.

9.5.2. Production Testing

Production testing is performed on every die post sawing. In this final test stage, the electrical performance tested data of all the dies shall be stored as well. The test data are relative to the specification to determine if the die is GOOD or NG. Occasionally due to outside fault conditions, testing yields could drop significantly for a prolonged period of time. Every effort should be made to investigate the causes of the drop in yields and to drive back to the normal range as soon as possible at all cost – headcount, overtime, and other resources could be deployed to the test floor, if warranted. The conditions need to diminish so the digging could be stopped after an abnormal test yield drop. This is normally done by setting a spec limit for the data set under question. In some very extraordinary cases, exploring the data to gain more insights into detailed patterns could be performed.

This is accomplished by segregating the data into a few bins (ranges) based on reasonable boundaries, and then some performance parameters are derived and plotted against the segregations to see if patterns could be observed. This activity is called “data exploration”. Ideally, each bin with good test data should have one to several contributing parameters that have differing values. A test by its name means excluding all the rejected patterns from further consideration. In this context, it somewhat becomes monkey’s business. In general, a good pattern is that for each designated die level good part, only that die in that bin has passed the test - in this case it is a good die and smartly developed test. Defect/NG patterns are split as evenly as possible in good bins.

There are no immediate needs to investigate further if nothing shows up in the main test variables. A deviation effect will be missed if the bad die level remains low, and it is possible that the test board may not be isolated from the disturbs, otherwise this should be flagged immediately. Packaging outlier parts due to external bad reflection or solder metal deposits on LIDD should be caught by the vendor subcons. There should be the first time to have the inference suspect believed otherwise to happen.

9.6. Conclusion

The degree of quality assurance, verification, and testing considered in the product life cycle will dictate the number of problems and the cost to resolve them. Manufacturers of leading-edge products may choose to be aggressive in the design cycle with regard to market success and delays to market. However, the use of high-risk technologies or trends can result in unforeseen problems, which can escalate into market disasters. A more moderate approach may be successful if the product is based on respected technologies and designs. Products of yesterday could likely become the leading-edge technologies and designs of the future.

The risk taken with a product defines its vulnerability to quality and reliability problems. A high-risk product will likely have a high number of problems but should also reap the benefits of high market value with a strong desired quality statement. The underlying argument is that the product and design should be carefully considered and history checked. A market-driven need exists for a new product to be developed, which cannot meet that need and so enters into a high-risk classification. Assuring that it has not been done before and that it will work is the only avenue to market value since there are no competitors.

Conversely, a medium- to low-risk product is built upon concepts of past design with some enhancements, or the technology is not leading edge and remains in a lower risk category. While new designs and concepts on second-generation technologies can also be high-value benefits, the capability of the product and its design ideas are easily known, which provides a lower vulnerability to market and product quality problems. Many drivers are in place when initiating product design, and care and consideration of the level of risk will define the potential market success and failure of that product. The latter can often be preempted with adequate testing and verification of the technology and designs used.

9.6.1. Emerging Trends

Advances in the semiconductor industries have ushered in an era of high technology and information. There is a surging demand for electronic products due to the rapid development of information technology. The semiconductor integrated circuits (ICs) can be categorized into standard ICs, designed by semiconductor manufacturers, and application-specific ICs, designed by customers. Semiconductor manufacturers expect the standard ICs to be low-cost, and therefore reduce the IC's size as much as possible. Moore's Law predicts that the chip's performance will double every 18 months. On the contrary, the design for testability (DFFT) requires the IC's size to reduce or increase the number of pins; thus, semiconductor manufacturers will lose the competitive edge in terms of cost and the need for new test equipment. Furthermore, cars are equipped with more and more electronic devices, and the scale of the automotive electronics market is getting larger. Zero-defect electronic chips are the industry's goal, and testing plays an essential role to ensure the reliability of crucial electronic products. However, the progress of IC testers lags behind that of semiconductor manufacturing: faster chips have been developed, but the capabilities of semiconductor test equipment have stagnated.

References

Cabanes, B., Hubac, S., Le Masson, P., & Weil, B. (2021). Improving reliability engineering in product development based on design theory: the case of FMEA in the semiconductor industry. Research in Engineering Design, 32, 309-329.

Hii, D. H., Muhammad, N. A., & Muhammad, N. (2024). Synergizing FMEA and PDCA for superior risk management and process improvement in the semiconductor industry: a case study. International Journal of Production Management and Engineering, 12(2), 180-194.

Sundaram, S., & Zeid, A. (2023). Artificial intelligence-based smart quality inspection for manufacturing. Micromachines, 14(3), 570.

Zhou, L., Zhang, L., & Konz, N. (2022). Computer vision techniques in manufacturing. IEEE Transactions on Systems, Man, and Cybernetics: Systems, 53(1), 105-117.

True, J., Xi, C., Jessurun, N., Ahi, K., & Asadizanjani, N. (2021). Review of THz-based semiconductor assurance. Optical Engineering, 60(6), 060901-060901.

Zheng, X., Zheng, S., Kong, Y., & Chen, J. (2021). Recent advances in surface defect inspection of industrial products using deep learning techniques. The International Journal of Advanced Manufacturing Technology, 113, 35-58.