Deep Science Publishing
https://doi.org/10.70593/978-81-989050-5-5_2

DeepScience
Open Access Books

Chapter 2: System-on-Chip (SoC) and Multi-Chip Module (MCM) innovations for compact electronic solutions

2.1. Introduction to SoC and MCM Technologies

The modern need to incorporate the maximum functions that can be integrated into a hardware platform while minimizing resource use, power consumption, and space taken is driving the continued rapid development of SoC and MCM technologies. The dense integration of SoCs combined with package-on-package type MCMs has led to very high-density heterogeneous packaging devices. Also, new chip stacking types such as 2.5D and 3D ICs are considered truly SoCs too. However, while SoC technology is unique and truly state-of-the-art compared with any other packaging or integration technologies, MCM technology is interdisciplinary and closely related to chip technology, packaging technology, assembly technology, substrate technology, and chip testing technology (Gupta & Mehta, 2025; Oliveira & Tan, 2025; Ramesh & Rahman, 2025).

Contrary to SoC technology, which is considered a specialty technology with a very unique process, some MCM technologies are considered mainstream technologies due to their individual features. For example, chip stacking and chip packaging have their own specialties and are used in most sophisticated electronic systems. These technological innovations help the consumer or market evolve. In this regard, MCM is a multi-chip type module with advanced functions and packaging technology capable of carrying out low-cost miniaturization, high connectivity, and low-power functions. They are commonly encountered in complex electronics such as automotive, medical, consumer, telecom, or computing systems. Additionally, with the acceleration of market demand, not only new designs, but also advanced packaging using old IC technology nodes must be commercialized quickly and economically. Thus, both SoC and MCM are essential to achieving good return-on-investment in tech business (Smith et al., 2025; Wang et al., 2025; Ramesh & Rahman, 2025).

2.1.1. Background and Significance

As electronics users, we are accustomed to continually getting better products, with more features at lower prices. When cells were first introduced into smart phones, they were primarily used for phone calls.

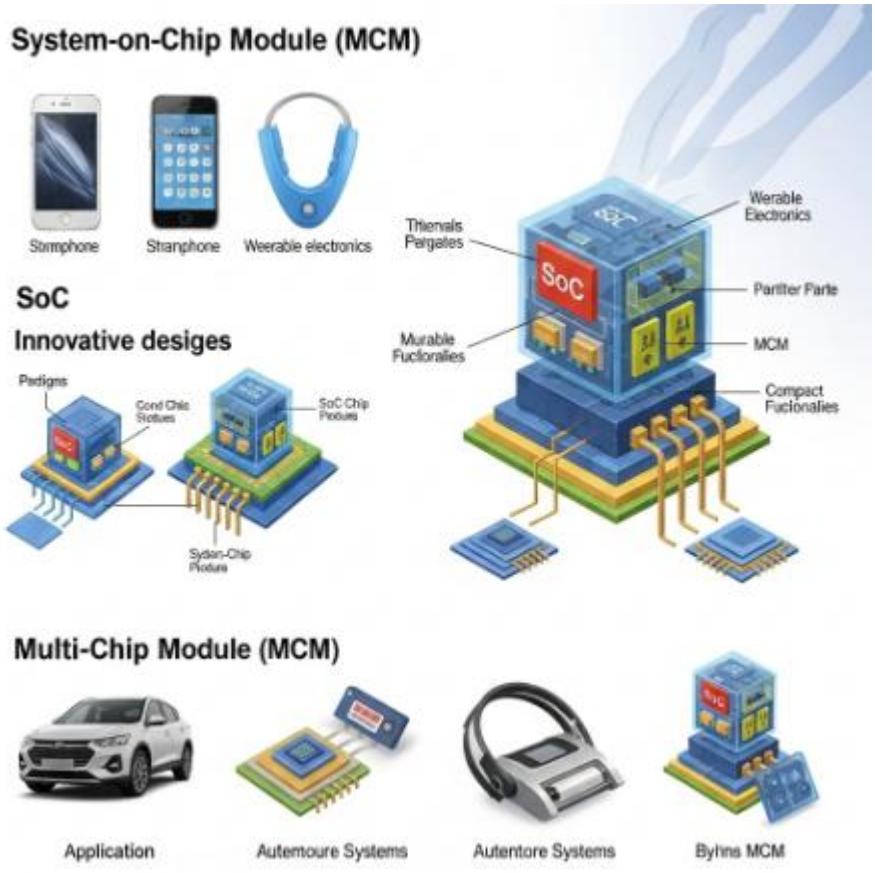

Fig 2.1: System-on-Chip (SoC) and Multi-Chip Module (MCM) Innovations for Compact Electronic Solutions.

Now, they are used for every form of communication and social media, as well as for GPS, cameras, music, and numerous apps. The only way that can continue is through innovation. A major part of the continued innovation is system-on-chip and multi-chip module technology. By integrating more functions, either on a single chip, or on a few chips combined into a module, overall size and capability improve, while cost is driven down. The increased integration enables the addition of advanced functions, such as facial recognition, artificial intelligence, simultaneous localization and mapping, with applications in autonomous driving, augmented reality, and introduction into original equipment manufacturers product lines, such as artificial intelligence for voice

interfaces, target tracking for security cameras, emotion recognition and voice analysis for customer insights in the business world.

Unfortunately, the innovation cycle continues to be shortened, so the time to bring a new or improved product to market is decreasing, while the complexity of the devices is rising, with developers trying to squeeze more and more functions into the same or decreased size. In this paper, we will focus on the technology and notation, to understand the role that system-on-chip and multi-chip module technologies play in allowing semiconductor developers to meet their market demands. The target applications are mainly consumer/communication market driven, illustrated by the major semiconductor companies, as well as pure-play foundries.

2.2. Historical Development of SoC and MCM

The history of MCM and SoC is a continuous interactive dialog between component integration and system design. The rivalry between MCM and SoC has always been an interesting journey that constantly pulls them together and then pushes them apart. A chronological account of significant developments and milestones is one way to view this dialog. Another wonderful lens to view this journey is the increasing pressure for enhanced performance and environmental compatibility imposed by various applications. A demanding application invariably spurs the search for creative silicon manufacturing solutions that make it possible to pack more functionality into a chip, and for innovative packaging concepts complemented by micro- and nano-fabrication processes that make it feasible to design systems using multiple chips integrated into a compact envelope. Accordingly, we first provide a chronological sequence of developments in MCM and SoC technologies punctuated by specific application demands, followed by an account of significant milestones. We conclude with a short summary of advances in important individual functions such as silicon, packaging, assembly, thermal, EMI, mechanical properties, design tools, and electrical performance. With this background, it is then easy to focus on the status and issues we face in sensors, actuators, display drivers, DSP, micro and Nano System controllers and engines, and a few other specific application domains. MCMs were the first to take off and SoCs, even at the risk of functionality and/or performance compromise, quickly followed to find niche elements of the MCMs in many applications.

2.2.1. Research Design

There are two basic approaches to research design. One can either adopt a quantitative or qualitative approach, or both, and select methods and contexts that best support the selected research approach. In seeking patterns of change and stability in SoCs and

MCMs, the historical narrative retelling the lives and stories of technologies is a useful method, establishing a sense of how these technologies have evolved or changed over time. In particular, it provides explicit contextual information. Brief details are given about the state of technology development at various historical time periods, about the commercial and international competitive conditions that governments and companies faced, about the relationship between companies and institutions during various historical time periods, about how SoC and MCM development plans emerged, and how investment decisions were made. Time lines explore the interrelationships among technological, market, investment, and firm capacity development in the development of SoCs and MCMs. The SoC and MCM time lines show specific emergence events and the timing of specific investments, and explore the relationship of these events and investments with major shifts in market demand and technology capability.

Such explicit establishment of a temporal context is generally absent from the quantitative approaches, which implicitly assume all empirical settings are similar. This retelling clearly shows that firms faced very different market conditions and technology capabilities at specific times over the last two to three decades. Thus, our specific rationale of employing a qualitative approach is to incorporate such rich contextual information into the analysis and to also explore in considerable depth the nature of the technology development process. However, not only is storytelling an attractive and natural way of relaying information, it is also indispensable for historical research methodology.

2.3. Key Components of SoC Design

Modern SoCs serve a spectrum of applications, ranging from ultra-low-power microcontrollers embedded in diverse devices to powerful microprocessors that run full-fledged operating systems. SoC accessibility has promoted the increasing demand for more capable, programmable, hardware features in small, low-cost packages. In this kind of application, the microprocessor is connected to several custom hardware accelerators for computation and multitasking purposes. With innovative and efficient homegrown solutions, chip vendors could support a palpable fraction of new consumer market trends. The versatility of portable computation in Smart Mobile Phones or Tablets have driven Tx level integration high, thus posing even more stringent requirements on power dissipation and, particularly, heat dissipation due to longer battery life and new designs that combine computation needs with optical or graphical features. Additional design challenges also arise by integrating logic circuitry with other functions, such as high-speed memory, high-speed I/O interfaces, and RF transceivers. These can create noise disturbances, impose timing constraints involving multiple die-to-die and chip-to-package interactions, and reveal reliability problems. Therefore, SoC design requires

more than merely implementing various functions utilizing the standalone techniques and tools meant for individual pieces of silicon. It requires the architectural exploration of the co-implementation of multiple functions on a single die, the creation of design tools and methodologies that support a die integration approach, product fabrication, and resulting product evaluation. There are several subsystems commonly implemented in SoCs. Microprocessors have been traditionally under the monopoly of few micromachinery vendors. They are the most complex digital blocks in large systems and are the only one capable of dynamically controlling program and data flow in the processing activities of any devices. Current microprocessors are fabricated with a large number of timber numbers of TX devices in a single die. The primary purpose of memory units inside the system is to provide data and code storage, and they hold information that is being processed currently, information needed in the near term future, and information that has been processed.

2.3.1. Microprocessors

Microprocessors are the essential core components of SoCs. The microprocessor fundamentally processes the data and controls the system, while the SoC platform supports the microprocessor functions in terms of system operating speed, internal and external interface connectivity, and compatibility with a range of peripheral devices, including memory systems. Companies in SoC design actively seek to develop faster, more powerful microprocessors capable of performing a wider range of tasks while simultaneously using reduced die area, lowering as far as possible the associated fabrication cost, thereby improving the yield per wafer. A key element in improving microprocessor speed is increasing the internal operating speed generally by means of clock speed increases made possible by faster transistor logic; dynamic logic circuits are commonly used to implement critical microprocessor circuits. Microprocessor functions are also implemented as parallel actions, with greater numbers of logic gates and wide microprocessor data paths made possible by increasing fabrication process capabilities, thus effectively reducing the overall number of circuitry clock cycles required for a particular operation.

In addition to improved microprocessor design parameters, the dominant trend in microprocessor design currently is the increasing concentration in a single microprocessor of functions originally specified by logic design engineers to be implemented in discrete chips on system boards designed by physical design engineers. The digital circuitry functions incorporated in microprocessors encompass a larger percentage of the total system functions. In addition to the standard arithmetic, logical, and general control functions, microprocessors incorporate peripheral functions for

controlling basic memory read/write, data transfer between the microprocessor and peripheral hardware, and various control functions.

A classic microprocessor architecture includes a central processing unit (CPU) that controls the operation of the system, which includes an internal bus or set of buses for intercommunication with the other operational chips in the SoC, and communication connections to interface with external devices. The CPU core can be implemented as either separate pieces of SoC circuitry that designate the logic gate function for executing the various tasks, or as a hard-coded structure for completing the actual computations via physical circuitry within the CPU. An instruction register, which holds instruction coding during its execution, and decoding logic that designates the resource operation performed with the data, are included as the inside circuits executed for each instruction cycle. Microprocessors may have designated, dedicated busses to handle specific microprocessor functions.

2.3.2. Memory Units

The microprocessor design, or System-on-Chip (SoC) – Multi-Chip Module (MCM) technologies, projects, and technologies must be integrated with key components. The components are: microprocessors, memory units, input/output interfaces. The memory unit stores the program and its data to be used to control the microprocessor timing. The stored data is generally read-out from the memory and sent to the microprocessor via a data bus and address decoder logic gates. The program instructions to be executed by the microprocessor are read-out, in parallel, from the program instruction memory, then fed to the internal microprocessor timing decision circuits.

There are two types of memory for the above-mentioned purpose. They are EEPROM and RAM. The former retains its content for a long time. Therefore, its stored data will be sent to the microprocessor once only at power-on time, and the microprocessor will work with this stored program until the power supply has stopped. The program in the latter is of temporary use, and can be written over repeatedly to the memory, either in parallel or serial mode, so that the program in the memory can be modified easily. These two types of memory have two different structures and peripheral circuits. The data and program stored in the memory, to control the internal timing of the microprocessor, are loaded from external memory by control commands of the peripheral circuit embedded in the SoC. In this section, we will discuss the design, technology, and advanced research of both types of memory, and also the peripheral circuits used with them for SoCs.

2.3.3. Input/Output Interfaces

Many embedded applications such as mobile devices, automobiles, and healthcare rely upon accelerated interaction with the physical world. In such applications, information is continuously exchanged through input/output operations, both internal-to and external-from the microprocessor computing engine. Microprocessors in turn rely upon I/O interface circuits to connect with uncommitted logic, standard library gates, and sensors. Through the application of device miniaturization, along with system integration trends noted in the early years of the 21st century, designers of circuit, logic, and sensor devices are no longer limited to discrete devices with their burden of connectivity, voltage, and noise margin scaling requirements. For such devices, SoCs may apply voltage scaling to mapped I/O interface circuits, thereby eliminating many of the drawbacks categorized with the pre-SoC solutions.I/O interfaces offer the same functionality and performance inherent to standard integrated circuit solutions, but have the advantages of single chip with advanced multi-chip packaging. Optimum solution sacrifices neither maximum bandwidth nor low power dissipation. In addition to being fine pitch, I/O circuits may also be tuned to drive specific resistive or capacitive loads. Very high speed I/O buffers for short communication distances may allow device input capacitances on the order of one tenths of a femtofarads with output driving strength approaching 0.7 to 1 ampere out of a supply voltage as low as 1.0 volt at speeds approaching the 130 to 180 picoseconds interface times measured on high performance microprocessor designs. Such speeds would allow for peak data rates on the order of 32 to 64 gigabits per second through 2 to 4 bit wide buses without the minimum energy dissipation as required for sustained communications through 16 to 32 bit I/O power comparable to high speed optical links while allowing the use of inexpensive noninvasive, electrical measurements for the sensor output signals.

2.4. Key Components of MCM Design

The advantages of MCMs come from their greater circuit densities and short interconnection lengths, which reduce both cost and electrical parasitics. However, MCM key components are more challenging than SoCs because they must support dissimilar functions and components from multiple technologies and they must be recycled from years of experience with larger board-level solutions. The fundamental building blocks of MCMs are the interconnect and supporting packaging solutions. These physically connect and assemble all of the disparate function die/tiles into a single module with high-density interconnects and good thermal management.

The interconnect technology determines the pitch of the MCM’s interconnect, which is the spatial density of traces/lines at which unique electrical signals can be efficiently connected from one component pad to another. The supporting packaging technology

establishes the thermal resistance and electrical parasitics as well as the lifetime reliability of the MCM interconnect. For a properly designed MCM, both the interconnect and the supporting packaging solutions must exhibit low microphonic sensitivity under mechanical shock loads to prevent dynamic gray-scale errors in sensitive optical processing MCMs.

The routing pitch, routing loss, and routing power of the MCM interconnect technology are the most critical technology tradeoffs, determining the overall circuit density and power dissipation of MCMs. The active interconnect bus, multilayer printed wiring available with thin-film deposition and photolithographic processes, is being optimized to exhibit the lowest routing pitch and routing loss. The routing pitch of MCM active buses may possibly match the lowest routing pitch of SoCs using new interconnect suggestions because shorter electrical signal lengths mean that the losses are much more acceptable compared to SoCs. In contrast, the routing power of an MCM is much greater than for a SoC because the physical thermal and residual stress solutions related to using dissimilar components on an MCM are both new and challenging.

2.4.1. Interconnect Technologies

The two dominant interconnect technologies enabling today's SoC design are copper wire and clock distribution network technologies. They are constrained by issues of performance, latency and power dissipation. Similarly, MCM interconnect technologies need to push the boundaries of integration, performance and power. The demand for smaller, lighter, low-cost products while maintaining performance and high productivity places a strain on the interconnects in both SoCs and MCMs. The active/capacitance area ratio of MCM wiring is significantly larger than for PCB wiring, hence area scaling pressures are not as great. Hence optical interconnect technology with its promise of enormous bandwidth and low power dissipation is likely to be adopted in the first instance for MCMs rather than SoCs. To put SiP/MCM interconnect integration density requirements in perspective we compare the wire integration density of MCM, SiP and SoC chips. MCM interconnects connect bare die to bare die, SiP interconnects connect bare die to package pads, and SoC interconnects route signals from sub-micron active regions to sub-micron active regions. A simple scaling of the number of SiP inner layers shows that the density of package to bare die interconnects for SiP is only 5 to 20% of that for MCM interconnects. Similar comparisons for SoC I/O pads show that, normalized to chip area, the density of device chip to substrate interconnections for SoC is only 3 to 10% of that for MCM interconnections. Once MCM interconnect density starts surpassing the limit beyond which further scaling is impractical, a more paradigm-shifting solution based on optical interconnects and novel SiP designs may be needed.

2.4.2. Packaging Solutions

Inclusion of components in customized packages is of utmost importance to achieve a higher level of integration in MCM technology. The first MCM products were assembled using advanced multichip carriers. While some of these products are still in production, they have been made virtually obsolete by flip-chip technology. Customized die packages with solder bumps on the chip edges allow the establishment of die-to-die solder connections. Designers are encouraged to develop circuits or systems as small as possible. Thus, chip area is minimized. For at least one dielectric spacer at the edge of the chips, bump-to-bump alignment accuracy of better than one micrometer can be achieved. A flip-chip mounted integrated circuit is usually directly attached to a printed circuit board. For a C-MCM, a customized MCM die, containing bumped devices, is connected to the hybrid PCB. Some present and future developments include assembly of MCMs using bumped dies on an FR-4 PCB. Flip-chip technology can also be used to package microwave or RF circuits including ASICs. Packaging designs with low inductance, shielding, and thermal management have been developed. Such packages become an SEP. Another important present trend toward subsystems and monolithic still in the future, is using ICs mounted in CoB on ceramic or silicon substrates. The CoB or C-MCM package can become a multi-chips subsystem or small multi-chip module. This package is a good solution for many future high-frequency, high-speed, or highly integrated circuits. The SSM can also be regarded as a conventional package used in the past for RF or microwave systems.

2.4.3. Thermal Management

Microelectronics thermal management is a technology that is critical in the evolution of multi-chip modules, as the power density is ever increasing. It is providing reliable access to emerging high-performance electronic systems in packaging and thermal-sustainability design—and realistic exploration within the architecture. The implementation of MCM will need a higher level of thermal management than nearly all SoC devices, and more dependence on thermal design. Cascaded packaging with ultra-thin layers is among the most compact and integrated packaging conceivable, and it can combine DA with microfluidic cooling, or other advanced thermal management. Flipped 3D and co-packaged devices reduce the distance heat must travel to be exhausted; and thermal dissipation microstructures built into the package allow expedient heat removal. Other specialized microchannel cooling methods appropriate for concentric devices reduce thermal paths, have no leakage surface, and are self-priming. But no specialized cooling is simple or performs better than external fin-cooling. More elaborate cooling requires a greater effort to either accommodate or override passive thermal modes and may disturb transients for synchronous designs. And still more elaborate thermal-

management techniques with large pump-dissipated power or disturbance are only useful for certain circuits under certain circumstances. For devices like ASICs that run only under certain conditions, specialized 3D cooling architectures or electrical methods are appropriate. More frequent use of passive-modes rely on the circuits addressing thermal relief and allow without needing the same level of design.

2.5. Advantages of SoC over Traditional Designs

Traditionally, many products consist of board-level designs requiring different integrated circuit (IC) chips to perform different tasks that the system demands. These particular chips are manufactured and designed separately and assembled on the board with surface mount technology or wire bonding. The typical building blocks of these board-level designs are discrete hybrid circuits like resistors, capacitors, inductors, filters, RF transceivers.

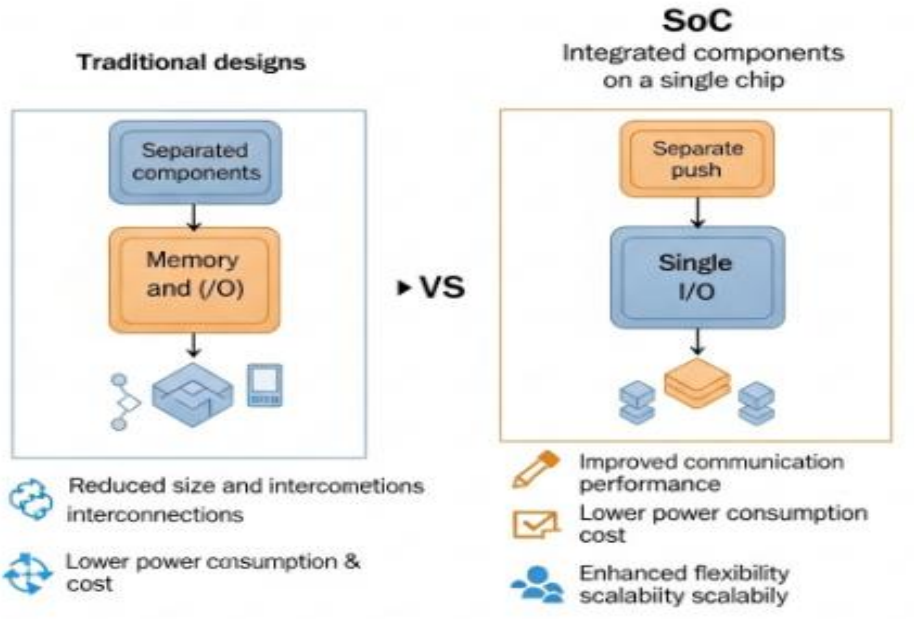

Fig 2.2 : Advantages of SoC over Traditional Designs.

The chips and boards are built specially to address a specific application problem at hand. With the advent of SoC technology, the functions, once needed to be placed in separate IC chips and assembled on a system board, are now being put together on a single chip in an SoC design. Various functions, both digital and analog circuits related to each other, are integrated together into a single substrate with a high degree of

optimization offered by the process technology and design capability. This has led to the miniaturization of the products, decreases in signal propagation delay, performance enhancement, and cost reduction.The reduction in chip area due to the use of SoC technology is the direct consequence of minimizing the interconnections between chips that are required in traditional board-level designs. Consequently, the amount of silicon consumed per module function is minimized. In addition, the modular cost reduction is realized with the integration of many submodules onto a single die for high-volume production tests. Assembly costs of the system are also reduced as some of the portions of the PCB are integrated and tested on the chip. In addition to size and cost efficiency, SoC designs generally consume less power than traditional designs because of the reduction in interconnections and lowered levels of input/output drive. These reductions in both chip size and power are directly associated with performance enhancements since power/size alleviates the heat dissipation requirements for physical configurations. Integration of independent functions and their interconnection through monolithic structures alleviate the noise interference issues of the signal pathways, thereby increasing the performance. The shielding techniques in SoC design may also further enhance performance.

2.5.1. Size and Cost Efficiency

Multi-chip modules are used to multi-package economically in a system-friendly way a number of standard or specialized chips that would otherwise be packaged separately in packages too large to place conveniently on the printed circuit board, thus utilizing space and area on the main PCB inefficiently. The growth in the number of devices per chip is large enough that about 5 chips with 512 or 1024 bits should eventually determine the square area of chips on a PCB. At the same time, the increasing failure rate per chip and the complications associated with realizing chips of non-standard function through custom design mask sets and services large enough to justify their costs on a significant number of chips leads manufacturers toward using CMOS technology to deliver SoCs with all the memory and logic – both analog and digital – that are sub-chips in SOCs today.

At the same time, the difficulties associated with the greatest yields at any layer of chip packaging or board assembly on what are in effect independent products in MCM manufacture through SoC manufacture are key drawbacks favoring SoCs. While MCMs can be realized by stacking thin chips of silicon or GaAs or by a process analogous to hybridization in which an epoxy sealant electrically links neighboring chips, the mechanical stability at high temperature diffusions and long term reliability associated at least with multi-level aluminum metal diffusion are restrictions limiting the application of chip stacking techniques to special cases of a few highly integrated chips

in MCMs. The reality that was noted earlier that SoCs combined with other standard chips in MCMs on a board with cheap inter-chip parasitics are often best means that MCMs with several SoCs and mixed signal chips are likely to dominate decade after decade. The fact that both SoCs and MCMs lead to PCB area reduction favoring MCM technology means that PCB area for neither technology is likely to decrease very much, which means that price per part needs to approach the price points of low cost separate chip making methods for either technology to be a practical method for a significant range of chips.

2.5.2. Power Consumption

A contemporary portable electronic device is demanding less power, while maintaining reasonable performance, owing to the fact that battery technology has not induced any significant fundamental change in the long-term, and reducing the battery capacity is not an option. Examples of such portable devices are: radio receivers, mobile phones, paging devices, laptop computers, which operate on a small rechargeable battery; wristwatches, cameras and certain IT applications, which operate on a small disposable battery; and hearing aids, which operate on a tiny rechargeable battery. These devices, therefore, work for a limited duration, thereby posing limitations on the size and weight of the battery pack, although fuel cells are being considered as a future solution. To make the task more challenging, the demand for performance of these devices is also increasing. Power dissipation is one of the limiting factors in the performance of all IC systems.

The portable battery – operated devices are not the only ones concerned with power dissipation. The intense power dissipation of high – density chip – sets in desktop and server applications has caused significant reliability problems in the past, along with the need for elaborate cooling techniques. With chips becoming faster and faster, the problems of heat dissipation are becoming more and more acute, sometimes seriously limiting performance. It need not be emphasized that the cost of power dissipation is very substantial throughout the world. So it is desirable to minimize dissipation not only in portable applications, but also in desktop, server, and other applications.

2.5.3. Performance Enhancements

Modern electronic systems often face conflicting demands from users for more and higher performance features on one hand, and for low power on the other. Customers desire to support higher performance multimedia services but become frustrated with products that consume so much battery power that they must often be recharged or replaced. The scalable System-on-Package architectural technology enables electronic manufacturers to meet these demands by integrating chips in parallel rather than in

series, distributing the power over several chips rather than stacking functions onto the limited area of a single chip, and thereby increasing density while maintaining compactness. Embedding chip-to-chip interconnects within packages while utilizing state of the art multi-chip module technology provides the area penalty, low power demand, and high thermal performance path that designers have previously been seeking.

The SOP design strategy offers many advantages over more traditional design approaches, enabling system manufacturers to put several already proven dies in packages while achieving significant cost savings and enhanced additional system features such as testability, flexibility, and higher bandwidth, lower latency connections between dies. In effect, the SoP does for packaging what SoC does for single chip designs. In addition, SOP provides a whole new level of design capabilities to electronic system manufacturers by allowing them to leverage off of other chip technologies that are otherwise incompatible with SoC technology. Consequently, SOP capabilities can also reduce time to market for new designs and/or proposed renovation approaches. It also extends the use of photo tooling and/or test capabilities. SOP technology-based products scale not only in performance but also in function and capability, and enable the mobile wireless world to deliver portable personal products that are multi-functional/enabled and compliant, while meeting user demands for more demanding low power at low cost.

2.6. Advantages of MCM in Complex Systems

Various design methodologies and fabrication approaches will be required as we move to higher and higher levels of integration. One method for combining technologies is to use silicon chip technologies to build modules and then package these modules together. This concept has come to be called multi-chip modules (MCMs) (or multi-chip packages). For a particular application, there may be several alternative approaches to integration. MCMs offer several important advantages over single-chip solutions. Most importantly, they overcome many of the fundamental physical limitations that constrain the performance of SOCs. Often, the same design technology, silicon process, and CAD tools can be used for both levels of integration. These advantages include:

1. Scalability. As transistor counts per chip increase and speed, power, or design area become issues, MCMs become a more attractive solution. MCMs allow for, in effect, an ease of scaling. For very complex designs in a maturing technology that require more than one silicon chip but may not profitably push the limits of integration, MCMs are an ideal solution. The system designer has the ability to design for performance, architectural complexity, low power, and low production cost independently of the design and fabrication details of a single chip by mapping the design onto chips with

appropriate functions that can be interconnected with a small amount of high density interconnect.

2. Flexibility. MCMs allow for greater flexibility than SOCs during the design evolution associated with silicon technology improvement, RTL design reliability, and RTL design experimentation. Rather than build a single function that may become outdated during the rapid silicon technology evolution of consumer electronics, MCMs allow for a complete product family at a single age that can be updated more rapidly with field programmable modules. Because design problems can be partitioned into MCMs rather than fixed upon a single-chip solution, disruptive errors concerning logic and circuit-level architectures can be repaired more easily.

3. Integration of Diverse Technologies. Certain systems will always require specialized circuits that cannot converge logically onto a single chip. MCMs will allow system designers to combine these circuit technologies using a single high-density packageable technology. MCMs will be particularly attractive for products where miniaturization is especially important — portable communications, consumer, biomedical, and military electronics.

2.6.1. Scalability

At the heart of the appeal of multi-chip modules and related packaging technologies is the concept of scalability, that is, the ability to take a complex system and implement it in a number of chiplets and other components and on a footprint that matches its ultimate technical and commercial value. Functionally-scaled system-on-chips are an important aspect of complex systems for a variety of reasons: they have the smallest possible area and volume and they bear the least possible cost-of-ownership at design time, at fabrication, and in the field. Placing system-on-chip designs that span too large a footprint on a single monolithic die "for the sake of integration" makes for heavy system design costs and for production yields that are too weak. Functionally-scaled SoCs also tend to perform better at lower power than their overly large brethren because of their modest internal interconnect complexities and relatively abundant pin resources.

While it is not strictly true, it is close enough to the truth to say that all major device technology advances have been driven by scaling advances. For many digital systems, chip scaling has persistently reduced circuit delays and parasitic resistances in scaling as much as possible in multiple technology generations before other physical factors become worse than the advantages from such scaling. Thanks in large part to the SCTP, it is now realistic to not only design large, complex digital systems from individual chips made using these scaled processes, but to be able to scale system designs economically

without being overly pinned down by module functions, packaging formats, and pin-assignment issues.

2.6.2. Flexibility

MCMs provide a flexible building block for the design of complex systems. Several simple, yet non-obvious, examples illustrate this point. By providing a layer of packaging, which accommodates circuit chips, which may or may not meet the full requirements imposed by the system, MCMs provide a certain amount of room for future development. Digital chips, in particular, are costly to develop but inexpensive to fabricate; as a result, digital MCMs may be implemented with parts whose technology is several generations older than the current state of the art. However, a digital MCM built around older technology is likely to be slower than the present generation. If the speed and/or cost of the MCM is low enough to justify the use of older circuits, then it becomes possible to fabricate the MCM more quickly, using it as a stopgap for those system applications that cannot be met by the current-generation circuits. In applications that require large numbers of MCMs, such as consumer products, the chance of having early design problems is greatly increased. In this case, the use of older circuitry in the MCM is an attractive option.

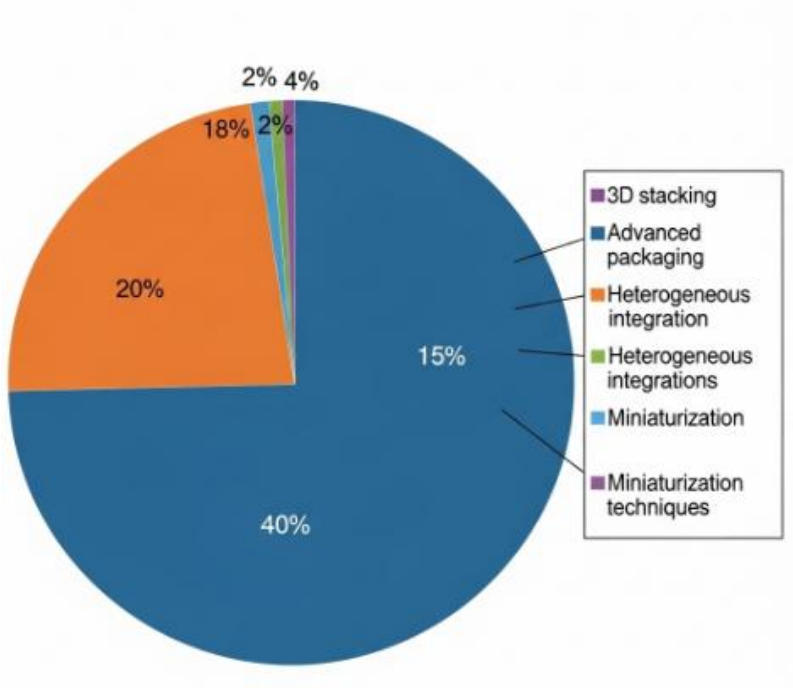

Fig : System-on-Chip (SoC) and Multi-Chip Module (MCM) Innovations for Compact Electronic Solutions.

Of all systems in which the technology support modules are MCMs, the systems that have real-time multitask monitoring and control functions are the most interesting. In this kind of system, real-time speed is required, and the time for system development and test is extremely short. If problems occur late in the electronics design and implementation cycle, the attempt to fix them in the technology support module reduces the probability of success. The best solution is to employ in the MCM a less expensive technology but use it to implement at least part of the task on a modular basis.

2.6.3. Integration of Diverse Technologies

One of the most prominent advantages of the MCM technology is that it can support the integration of the multiple technologies that are typically found in the type of complex system discussed. Very custom digital circuits, D/A and A/D converters, high-frequency circuits for RF and microwave signals, optical components, sensors, analog components, MEMS circuits, and power management circuits are just many of the types of functions that can be integrated in a single module. The module may be partitioned so that parts of it are implemented in different chip technologies, leading to coexistence of ASICs, custom ICs, and other chips in one MCM product. The ability to support the different interconnect technologies necessary for each chip technology, in terms of the semiconductor die preparation, chip packaging and module interconnect routing, in a single module permits the lowest-cost solution for a complete system.

In many cases, commercial systems require a variety of supporting components and functions around the primary core processor chip. These supporting functions may be available as chips offered by silicon vendors. The cost of the supporting chips seldom makes a system design business case attractive. However, there are systems that support products which use a relatively small number of units, yet have a high dollar value. Those systems present a business case for custom implementation of the supporting functions as chips. A MCM with embedded passives also supports a persistent demand for ICs with added functionality in miniature size for performance-sensitive, portable systems.

2.7. Conclusion

This work examines the major advancements that have taken place in microelectronics over the last twenty years, and how these advances make it possible, and even likely, that heterogeneous integration of multiple dies into system-on-chip and multi-chip module devices will continue to grow and prosper as chip integration technology advances. Chip integration technology has been propelled further by the tremendous growth in computing and communications that has occurred over this time, along with the equally extraordinary increase in the quantity of data that the world generates in

nearly all aspects of modern life, the so-called big data revolution. Commercial and military demand for dramatically larger computing power is fostering innovative integration of silicon multi-chip modules or system-on-chips with microscale and nanoscale optoelectronic and photonic devices, RF functions, MEMS, NEMS, carbon nanotube optoelectronics and interconnects, and reconsideration of artificial molecular devices, among others. The goal is to achieve clear functionality at the microscale and nanoscale, while at the same time achieving high performance job processing, low energy consumption, and low cost through massive parallelism for proper applications, when executing large-requirement tasks in order to seamlessly interface with the cloud. Miniaturization and packaging of microscale and nanoscale chips must proceed in parallel with the high performance and low energy consumption goal. Today the term Moore's Law is still being applied at longer time intervals, as it becomes more and more clear that the general idea of steep scaling down of minimum feature size is still applicable for massively integrated digital devices.

Time has come for reconsideration of high volume, low cost integration of multi-chip modules and system-on-chips utilizing multi-die integration in various ways, as advanced CMOS is applied, especially for larger application domains for incorporating computation devices and the required sensors, actuators, and other specialized functional chips. Memory bound applications have reduced the need for scaling down, and have stimulated demand for alternative solutions that deal with the restrictions of current CMOS scaling technology. The utility of heterogeneous system-on-chips and multi-chip modules for a diversity of device applications, including implementation of the Internet of Things and microsystems, is evident.

2.7.1. Future Trends

As well as Moores law continues to hold strong we will continue to see scaling and integration increase SoCs are becoming more complex both in the number of functions they integrate as well as the number of chips that can be bundled onto a single package Multi-chip packaging will have product duty cycle advantages and die cost advantages as older and higher cost nodes reach end of life and need to be replaced with newer device technologies New device technologies are moving from exotic approaches to cost effective commercial available solutions Technologies such as GHz integrated RF transceivers are shipping on low cost processes When Systems in Package technology and associated packaging will become fully compliant with semiconductor device manufacturing information will become a reason of focus migration and act face no cost and technical obstacles The important enabling methodologies will be design tools and a package design tools database for parameters such as crosstalk resistance and redundancy helper utility for SiPs is provided in a package design tools database of

critical parameters such as crosstalk resistance redundancy helper utility for high performance SiPs work in SoC SiP integration and in semiconductor SiP characterization had successful early effort of SiP migration in the early Design packages because of density economies of scale consolidate months for Wireless and Multimedia Products is expected that composite growth SiP annual average revenue will be expected up over between 2002 and 2005 above their substantially is needed it develop Multi Chip Module technology into a consumer driven budget as flash memories technology Multi-DIech Wafer Wafer integration packages versatility of Silicon On Insulator and enabled cheap compressors for after years of prototypes are needed arrive at products with economics serializers drive available products and wireless trigger digital bridging for micro sensors Integrated Networks have focused products available.

References

T. Wang et al., "Millimeter-Wave Circuits for Beyond-5G Wireless Front-Ends," IEEE Microw. Mag., vol. 26, no. 1, pp. 67–75, Jan. 2025.

N. Gupta and R. S. Mehta, "Efficient FPGA Implementation of Adaptive Beamforming Algorithms," IEEE Trans. VLSI Syst., vol. 33, no. 2, pp. 303–312, Feb. 2025.

E. Oliveira and L. Tan, "Energy-Aware Circuit Design for Neuromorphic Systems," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 44, no. 5, pp. 870–881, May 2025.

D. Smith et al., "AI-Assisted Optimization in RF Transceiver Circuitry," IEEE Trans. Microw. Theory Techn., vol. 73, no. 6, pp. 1290–1301, Jun. 2025.

V. Ramesh and M. A. Rahman, "An Ultra-Low Latency Wireless Protocol Stack for Smart Manufacturing," IEEE Trans. Ind. Informat., vol. 21, no. 3, pp. 765–776, Mar. 2025.